DESIGN AUTOMATION CONFERENCE

KEYNOTES

Sponsored by: MAGMA

MONDAY
JUNE 6 @ 2:00 - 3:00pm

UP CLOSE AND PERSONAL WITH STEVE WOZNIAK
Steve Wozniak
Fusion-io

TUESDAY
JUNE 7 @ 8:30 - 10:00am

MEGATRENDS DRIVING EMBEDDED MULTICORE INNOVATION
Lisa Su
Freescale Semiconductor, Inc.

WEDNESDAY
JUNE 8 @ 11:00am - 12:00pm

THE IMMINENT EDA TRANSFORMATION
Gadi Singer
Intel Corp.

THURSDAY
JUNE 9 @ 11:00am - 12:00pm

COGNITIVE COMPUTING: NEUROSCIENCE, SUPERCOMPUTING, NANOTECHNOLOGY
Dharmendra S. Modha
IBM Research

TECHNICAL PROGRAM HIGHLIGHTS

ONLY THE VERY BEST

The technical program has an exceptional quality of over 156 presented papers, 44 technical papers/panels and 10 special sessions tailored for researchers, developers design and system engineers along with management in the electronic design, design automation and embedded systems industry.

DESIGN MEETS AUTOMATION

FOR MORE DETAILS VISIT:

www.dac.com

Sponsored by:

Apache

USER TRACK FOR EDA USERS, BY EDA USERS

- System-Level Design, Modeling, and Validation
- Tuesday User Track Poster Session
- Case Studies in Systems and Software
- Timing is Everything
- Ultra-Deep Sub-Micron Physical Optimization
- Wednesday User Track Poster Session
- New Frontiers in Power
- Real-World Functional Validation
- Embedded Systems and Software
- Thursday User Track Poster Session
- Case Studies in Formal Verification
- Advanced Circuit Design Techniques

Management Day

Sponsored by:

SYNOPSYS®

THE EDGE OF BUSINESS AND TECHNOLOGY

Tuesday, June 7

Management Day is focused on issues at the intersection of business and technology, and is specifically directed to managers and decision-makers.

ESS Executive Day

Wednesday, June 8

The ESS Executive Day is dedicated to bringing industry stakeholders together in one room to shed light on where SOC design is headed.

EXHIBIT FLOOR

ALL OF DESIGN AUTOMATION UNDER ONE ROOF

SUNDAY KICK-OFF RECEPTION

Co-Sponsored by: IBM, 48 DESIGN AUTOMATION CONFERENCE

3 COCKTAIL RECEPTIONS

6:00 - 7:00pm in the Center Terrace

Monday

Co-Sponsored by:

Apache

ARM

Tuesday

Sponsored by:

ATRENTA

Wednesday

Sponsored by:

48 DESIGN AUTOMATION CONFERENCE

EXCITING EVENTS

Monday - Wednesday

9:00am - 6:00pm

- 175+ Vendors
- New Products and Services
- Exhibitor Forum
- ESS Zone
- Embedded Theater
- Exhibits Free on Monday

PAVILION PANELS

Sponsored by: GLOBALFOUNDRIES

- Gary Smith on EDA: Trends and What's Hot at DAC
- Teens Talk Tech: You Don't Know Jack
- Hogan's Heroes: The Re-Aggregation of Ecosystem Value
- Town Hall: What EDA Isn't Doing Right
- C-to-FPGA Tools: Ready for the Mass Market?
- 3D IC: Myth or Miracle?
- Career Velocity Vectors: The Excitement of Engineering
- Words of Wisdom: A Conversation with the Marie R. Pistilli Award Winner
- Pistilli's Perspective: EDA Future – Feast or Famine?
- Stop That Thief! – IP in Global Markets
- Verification: What's in Your Wallet?
- Why the Delay in Analog PDK?
- Multi-Core: Madness or Just Today's Chaos?
- High Level Synthesis: What Works?
- 3D Extraction: Coming to a Design Near You?
- Low-Power Report Card: Are We Cool?
- Android, MeeGo, and Linux: Where Is It All Heading?
- IPs and FPGAs: Where's My Free Lunch?

Platinum Exhibitors

GLOBALFOUNDRIES

Mentor Graphics

SYNOPSYS

Gold Exhibitors

Apache

MAGMA

tsmc

Silver Exhibitors

ATRENTA

cadence

SpringSoft

accelerating engineers

TECHNICAL PANELS TECHNOLOGY SMACKDOWN

- Hackers and Attackers: How Safe is Your Embedded Design
- Crystal Ball on Low Power: Limiting Trends and Strategic Solutions
- Cloud Computing and EDA Forecast: Sunny Skies or Storm Clouds Ahead?
- EDA Research: Stalled, Driving in Circles, or Running out of Gas?
- Software-Hardware Verification Battle: Prototyping vs. Emulation
- The Billion Dollar Question: How to Verify Billion-Gate Designs
- ESL HW/SW Verification: A Reality Check
- 3D: Devils, Details, and Debate
- Double Trouble or Double Your Fun: Double-Patterning and Variability
- In IP We Trust: IP and SoC Verification
- Parallel or Paralyzing: Is Parallel EDA Worth the Trouble

TUTORIALS LEARN AT DAC, DESIGN TOMORROW

- Android Apps Development Boot Camp
- iPhone Apps Beginner Guide
- A Designer's Guide to Sub-Resolution Lithography: Enabling the Impossible to get to the 15nm Node
- Demystifying TSV-Based 3-D Stacked ICs - A Design and Test Perspective
- System-Level Design and Software Development for Energy Efficient Platforms: Challenges from Models to Methods
- Starter Kit for Chip to System Reliability

WORK-IN-PROGRESS (WIP)

Wednesday, June 8 @ 6:00 - 7:00pm in the Sails Pavilion

In contrast to other sessions at DAC, this session aims to provide authors an opportunity for early feedback on work-in-progress or to share early results.

SAN DIEGO CONVENTION CENTER

San Diego, CA USA
JUNE 5-9, 2011

Sponsored by:

SIGDA special interest group on design automation

CEDA IEEE Council on Electronic Design Automation

EDA CONSORTIUM

In technical cooperation with:

SSCS