

? Platinum Exhibitors ?



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accelerating engineers

Listing as of May 12, 2011

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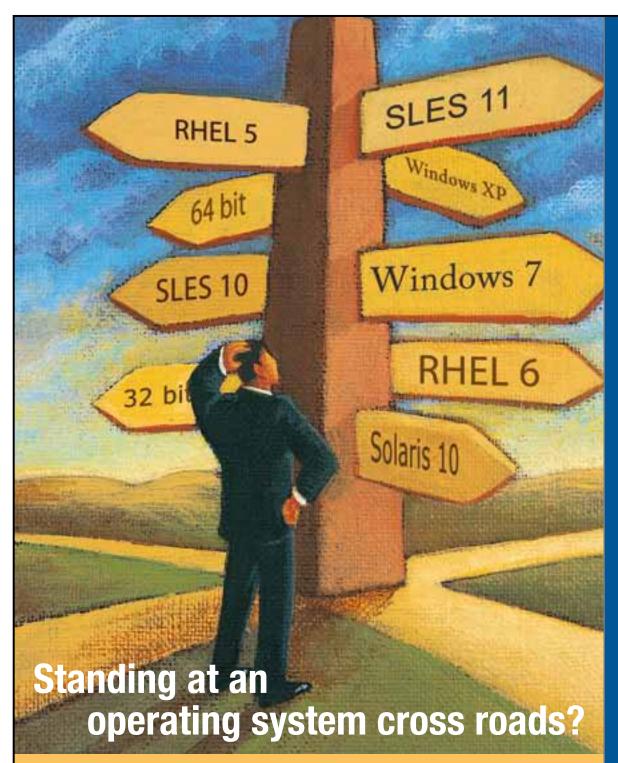


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IP SoC VILLAGE

BOOTH 1915

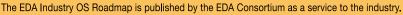
Design and Reuse
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IQ-Analog
L & T Infotech
MoSys Inc.
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Silicon-IP, Inc.
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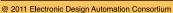


Need to know if your operating system will be supported by your Electronic Design Automation (EDA) supplier?

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• Workshop for Women in EDA



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Magma Design Automation, Inc.



Mentor Graphics Corp.

- Exhibition Rest-Stop



- Management Day
- Food Court



True Circuits

Aisle Signs

Booth: 2830

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Accelicon Technologies, Inc.

Cupertino, CA

www.accelicon.com

Accelicon Technologies, Inc. (Accelicon) is the leading provider of device-level modeling and PDK solutions to the semiconductor industry. Solutions include MBP for SPICE model generation, MQA for SPICE model validation and AMA for sub-45nm design and model analysis. Accelicon, founded in 2002, serves over 100 customers throughout the world. For more information, visit http://www.accelicon.com

ACML / 2 WCL

Lannion, France

www.2wcl.com

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World's First Online Library For ECAD, MCAD, 3D and Thermal Models Released by Automatic Component Model Library (ACML)

Automated Component Model Library (ACML) is the first web based company proposing a complete solution to automatically create ECAD, MCAD, 3D and Thermal libraries from a datasheet (available in all ECAD or CAD formats on www.2wcl.com).

ACML provides electronic component modeling automation including the ability to allow the use of customers specific Design Rules.

With the implementation of the first worldwide online library, ACML solution is allowing integration of mechanical and electrical components in Mechatronic.

The software solution package is intended for everyone in the electronics industry: semiconductors manufacturers, semiconductors users and printed circuit board professionals.

Please visit www.2wcl.com

Agilent Technologies

Santa Clara, CA

www.agilent.com

Agilent EEsof EDA (booth #1229) is the technology leader and industry's leading supplier of Electronic Design Automation (EDA) software for microwave, RF, high-frequency, high-speed, RF system, electronic system level (ESL), circuit, 3-D electromagnetic, physical design and device-modeling applications. Join Agilent in booth #1229 where you can look at the most trusted tools for highly integrated RF circuit simulation and analysis as well as Communications ESL. Come see the latest in:

- GoldenGate RFIC solutions
- SystemVue Communications ESL

Aldec, Inc.

Henderson, NV

www.aldec.com

Aldec has been delivering advanced design verification and robust debugging technology to the hardware engineering community for over 25 years.

Booth: 1243

Booth: 1714

Booth: 2749

Booth: 2114

As a global EDA company, Aldec offers industry-proven tools to address design verification challenges with high-quality products such as:

- Active-HDL (simulation/debugging for FPGAs),
- Riviera-PRO (UVM/OVM based high-end verification methodologies for large ASIC and FPGA designs),
- ALINT (design rule checking),
- SFM (grid-based regression manager),
- HES (simulation and acceleration),

We invite you to sign up for a private Technical Session at a time that is convenient for you: http://www.aldec.com/dac48

Altair Engineering

Troy, MI

www.altair.com

The PBS Works™ suite of tools allows enterprises to maximize ROI on computing infrastructure assets: making engineers more productive and making your infrastructure more efficient, more reliable, and more cost effective. PBS Professional® optimizes use of hardware and expensive software licenses; and PBS Analytics™ enables data-driven planning, chargeback, and forecasting. With a 25-year-plus track record, Altair has provided innovative solutions delivering sustained competitive advantages to our 3,000+customers throughout the world.

Altos Design Automation

Campbell, CA

www.altos-da.com

Are you ready for more corners? Altos Design Automation (www.altos-da.com) provides ultra-fast, very easy to use IP characterization solutions for standard cells, complex I/Os and embedded memory. With Altos' "inside view" technology additional library corners complete with timing, noise and power (CCS/ECSM) can be created in hours not days. Altos also offers library validation, statistical timing model and AOCV table creation. To learn how to "improve your view" and get the library corners you need fast, visit our DAC booth.

AMIQ EDA

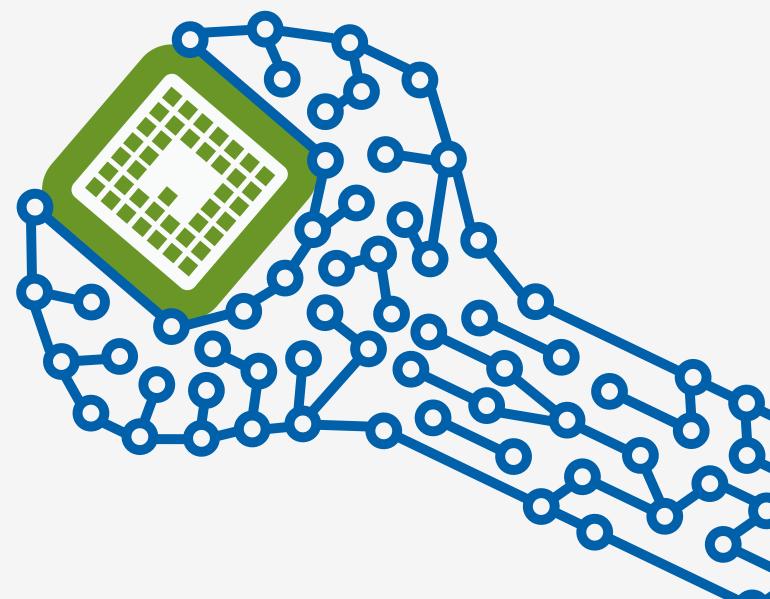
Bucharest, Romania

www.amiq.ro

AMIQ EDA provides Design and Verification Tools (DVT), the first integrated development environment (IDE) for the hardware design and verification languages Verilog, VHDL, e, and, SystemVerilog. Created to maximize design and verification productivity, DVT enables efficient code writing and simplifies legacy code maintenance. It comprises an IEEE standard-compliant parser, a smart code editor, and a complete suite of tools for code navigation and analysis. DVT integrates with all major simulators and supports verification methodologies like UVM, OVM, and VMM.

Websites: www.amiq.ro; www.dvteclipse.com

Contact: etools@amiq.ro



Your New Toolbox

Now integrated development environments (IDEs) that are popular in the software industry can make a difference in hardware design and verification too.

DVT

Be a step ahead and update your toolset with Design and Verification Tools (DVT) — a powerful, yet easy to use IDE for SytemVerilog, e, Verilog, and VHDL. Write code more efficiently, simplify debugging, navigate with ease through complex projects, automatically check verification methodology compliance, and much more.

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Learn more at: www.dvteclipse.com

AMIQ J

Booth: 3016

Gold Exhibitor

Booth: 2448

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AnaGlobe Technology, Inc.

Hsinchu, Taiwan

www.anaglobe.com

AnaGlobe focuses on the field of innovative IC physical layout design software and upgrades an efficient and time-saving work flow solution. Our products include:

Thunder (supports GDS/OASIS/OpenAccess/LEF/DEF) is huge capacity chip level layout integration, consolidation, and debugging tool with 10X performance gain.

GOLF (OpenAccess-based) is the next generation PCell design environment that provides intuitive GUI to easily define a PCell on an existing layout directly. GOLF can also integrate user-defined OA objects into PCells written in TCL/Python/Perl and C++ with OA native API.

Apache Design Solutions, Inc.

San Jose, CA

www.apache-da.com

Apache Design Solutions, Inc. is a leading provider of innovative power analysis and optimization solutions that enable the design of power-efficient, high-performance, noise-immune ICs and electronic systems. Apache's comprehensive suite of integrated products and methodologies advances low-power innovation and provides a competitive advantage for the world's top semiconductor companies. The company's differentiated software solutions help lower power consumption, increase operating performance, reduce system cost, mitigate design risks, and shorten time-to-market for a broad range of end-markets and applications.

Applied Simulation Technology

San Jose, CA

www.apsimtech.com

Applied Simulation Technology provides solutions for the modeling and simulation of Electromagnetic effects for PCB, IC, IC packaging interconnects and power delivery systems. EMI, Signal Integrity and Power Integrity for high speed designs are the major focus of the product offering. Apsim has been an innovative leader in this area since 1996. The products are well integrated into industry standard CAD progams and designed to fit into demanding design flows without compromising the capabilities, accuracy and flexibility Engineers demand.

ApS Brno Ltd., Codasip Division

Brno, Czech Republic

www.codasip.com

The Codasip® is dedicated to help the customers to develop MPSoCs using ASIP cores more efficiently while reducing the time-to-market significantly.

Based on the user requirements, Codasip® provides a solution in form of the retargetable tools for programming and simulation together with fully synthesizable hardware representation. The Codasip® provides as well EDA tools for HW/SW co-design together with a virtual platform for a fast prototyping on the system level. In the early design stage, the Codasip® team can prepare a model of the costumers MPSoC.

ARM, Inc.

San Jose, CA

www.arm.com

ARM designs the technology that lies at the heart of advanced digital products, from wireless, networking and consumer entertainment solutions to imaging, automotive, security and storage devices. ARM's comprehensive product offering includes 32-bit RISC CPU and GPU, software, standard cell libraries and memories, connectivity products, tools and training services, supported by the industry's broadest partner community. http://www.arm.com.

Booth: 1323

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Booth: 2125

Artwork Conversion Software, Inc.

Santa Cruz, CA

www.artwork.com

Artwork will be demonstrating our software tools for viewing and processing GDSII/OASIS files including boolean, sizing, fracturing, plotting and extracting. We'll be showing translators for GDSII, OASIS, MEBES, AutoCAD, ODB++. SolidWorks, Cadence and other EDA databases.

We will also be showing new interfaces from EDA programs into the 3D CAD world, ideal for modeling and simulating stacked die and advanced IC packages.

ASICServe LTD

Modiin, Israel

www.asicserve.com

ASICServe Ltd. is a leading supplier of ASIC design and verification services used by companies worldwide. The innovative solutions provided by ASICServe allow customers to manage and achieve results in the quickest possible way. ASICService software suite includes:

- BOOSTAR™ comprehensive and fast path to ASIC STA verification and timing closure.
- WAVSTAR™ eye-opener waveform representation of ASIC timing constraints and reports.
- VECOOL® ECO language for fast ASIC ECO implementation.
- VP™ Management and Control interface to best-in-class ASIC tools.

Asvan

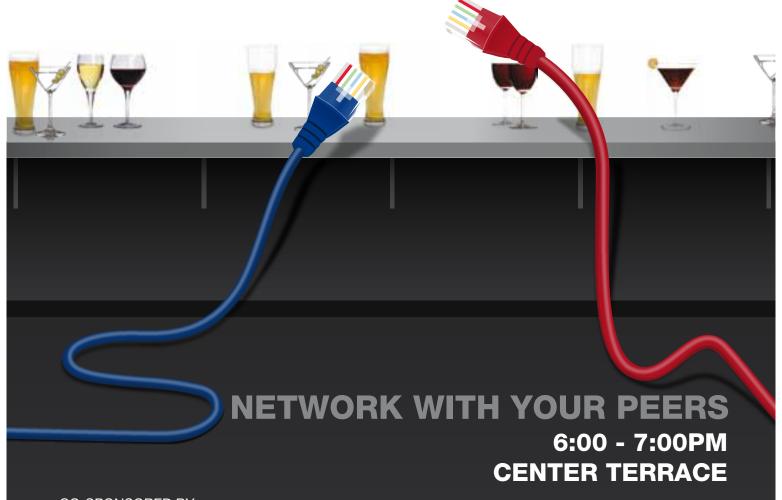
Montbonnot, France

www.asygn.com

Asygn is a Grenoble-based startup, specializing in the design and verification of analog/mixed-signal and RF systems. The company delivers application-focused solutions in order to deal with tough issues that traditional, generic approaches cannot handle. Asygn's solutions incorporate their own analog system level simulators, which provide major performance advantages. The company has had notable successes in the following applications: imaging arrays; mobile phone radios; MEMs and NEMs sensors; digital and fractional PLLs; high speed IOs.



MONDAY COCKTAIL RECEPTION



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ARM

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Silver Exhibitor

Booth: 1643

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ATEEDA

Edinburgh, United Kingdom

www.ateeda.com

ATEEDA lets you solve SoC test cost, time and access problems. Cut your ADC or DAC test costs by 90% using our EDA tools to configure our tiny, silicon-proven Built-in Self-Test IP. Fast, accurate on-chip analog testing - in parallel - even when access is restricted. Whether you have SoC, SiP or AMS test issues, we have the solution. ATEEDA - Cutting the cost of analog test.

Atoptech

San Jose, CA

www.atoptech.com

ATopTech was founded by leading EDA physical design implementation experts to build the next generation of place and route tools focused on designs at 65nm and below. Our goal is to provide the fastest turn-around time while providing the best quality of results. AtopTech's products form a complete netlist-to-GDSII physical design solution, from top level design and prototyping to complete block level design while handling all the complexities of variability such as MCMM and AOCV. Excellent correlation with both timing and physical verification sign-off tools is one of our trademark capabilities!

Atrenta Inc.

San Jose, CA

www.atrenta.com

Atrenta provides comprehensive solutions that allow software, semiconductor IP and advanced process technology to be combined in a predictable, convergent, cost-efficient manner to create the World's most advanced SoC devices. Automated and interactive SoC assembly, rigorous IP qualification, extensive RTL optimization for power, timing, test, clocks and routing, as well as links to embedded software, are all part of Atrenta's SoC Realization

solution. A solution that bridges the gap between system-level

design methodologies and traditional silicon implementation tools. Atrenta, the SoC Realization company.

Ausdia Inc.

Sunnyvale, CA

www.ausdia.com

Frustrated by timing constraint issues found in implementation? Concerned that incorrect constraints might result in a silicon respin? Ausdia has developed a revolutionary software solution, Timevision, that can eliminate these problems. Timevision automates the creation and verification of timing constraints throughout the design hierarchy. It works either from scratch or incrementally, and at RTL or gate-level netlist level. Timevision is architected for more than 500M gate designs and 1000s of clocks, and is silicon-proven technology.

austriamicrosystems

Raleigh, NC

www.austriamicrosystems.com

austriamicrosystems is one of the world's leading manufacturer of advanced analog/mixed signal IC's using process technologies like High-Voltage CMOS, BiCMOS, and SiGe-BiCMOS. With superior support, austriamicrosystems succeeds to be an attractive analog foundry partner especially for fabless design houses. In addition to wafer production services, we offer extended foundry support including design-support, analog process-characterization, wafer probe, and final test. Visit www.austriamicrosystems.com for more information.

Booth: 2327

Booth: 1605

Booth: 3320

Avery Design Systems, Inc.

Andover, MA

www.avery-design.com

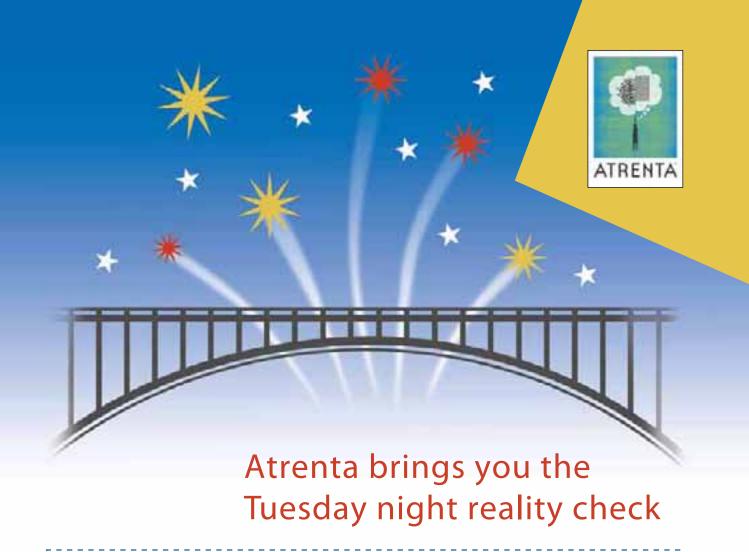
Avery is a leading provider of intelligent functional verification solutions. Insight offers effective early RTL formal verification including automatic microarchitecture-level assertion and coverage synthesis, X verification to find non-determinism problems in regular and low power designs, and RT-level DFT analysis for atspeed path delay fault and small delay defect coverage estimation and automated RTL repair. Proven VIP for PCI Express, USB, xHCI, UAS/BOT, AXI3/AXI4/AHB, and SATA with robust models, protocol checking, and compliance testsuites. SimCluster parallel simulation accelerates RTL and gate-level simulation by 5-10X while leveraging industry leading simulators.

Axiom Design Automation

Milpitas, CA

www.axiom-da.com

Axiom will showcase MPSim, the state-of-the-art, industry proven high performance Verilog and SystemVerilog simulator. MPSim comes integrated with the most advanced debugger, compiled testbench automation including OpenVera, multiple clock domain verification and comprehensive coverage analysis for quick verification closure. MPSim is fully compatible with existing Verilog environments and supports, OVM, VMM, UPF, UVM and SystemC. Please come and see us at Booth 3320 and find out for yourself about several companies who have cut down their verification cost by taping out highly complex chips exclusively with MPSim.



By Tuesday night at DAC you're tired of all the hype and promises. Time for a reality check and something new.

The SoC reality is that the gap between the System Realization and Silicon Realization, or EDA Classic, must be bridged.

SoC Realization is what you're searching for. Robust RTL, quality IP, automated assembly and links to software finally complete the flow.

Whether it's power, clocks, test, constraints or congestion that keep you up at night, you need an SoC Realization solution that is....well...real.

Join Atrenta as we celebrate the emergence of true SoC Realization.

No hype, no promises. Just the real deal.

Plus, free wine & beer. Really.

Tuesday, June 7, 2011, 6:00-7:00pm - Center Terrace at the San Diego Convention Center

ATRENTA, The SoC Realization Company

Booth: 2431

Booth: 3149

BEEcube, Inc.

Fremont, CA

www.beecube.com

BEEcube provides High-Speedmultiple FPGA prototyping and development platforms. BEEcube will be announcing a new product. With over 150 BEE systems purchased world-wide, BEE4technology targets:

- · Computation/Algorithm prototyping
- High Performance Computing (HPC)
- High-end Signal Processing applications MIMO, Radar, SDR, and SignalIntelligence

BEE Systems Offer:

- · Direct DAC/ADC interfaces,
- Symmetrical Honeycomb™ architecture
- High-speed Gigabit Sting I/O™,
- Monitoring/Control with Nectar OS ™,
- Industry's largest Trace memory 128GB.

BEEcube Platform Studio $^{\mathsf{TM}}$ (BPS), a hardware/software codevelopmentenvironment on top of MathWorks Simulink $^{\mathsf{TM}}$ framework, along with IP-Stitcher $^{\mathsf{TM}}$ allows Easy Algorithm deployment without any RTL knowledge.

Berkeley Design Automation, Inc.

Santa Clara, CA

www.berkeley-da.com

Berkeley Design Automation, Inc. is the recognized leader in nanometer circuit verification. The company combines the industry's only unified verification platform, Analog FastSPICE, with exceptional application expertise to uniquely address nm circuit design challenges. Over 100 companies, including most of the World's top 20 semiconductor suppliers, rely on Berkeley Design Automation to efficiently verify their nm-scale circuits.

Blue Pearl Software

Santa Clara, CA

www.bluepearlsoftware.com Booth: 1035

The New Blue Pearl Suite features an integrated Visual Verification Environment to easily create and visualize timing constraints, view clock domain crossings, and intelligently manage RTL debugging messages. Blue Pearl's next generation technology integrates rapid design analysis, CDC checking and timing constraint generation into a single tool which operates in a native Windows or Linux environment. Blue Pearl's technology, which is based on rapid RTL abstraction and symbolic simulation technology, analyzes designs in orders of magnitude faster than competitive tools, producing more accurate results.

Bluespec, Inc.

Framingham, MA

www.bluespec.com

Bluespec is the Synthesizable Modeling Company™. With Bluespec, models and testbenches can be synthesized along with legacy IP to employ emulation much earlier for modeling, verification and early software development. Bluespec makes emulation much easier, more affordable, and deployable from concept to volume silicon. Bluespec provides a synthesizable modeling kit and emulation infrastructure, all powered by the only general-purpose, high-level synthesis toolset for any use model (models, testbenches, production IP) and design type (datapath, control, interconnect).

Breker Verification Systems

Austin, TX

www.brekersystems.com

Breker, The SoC Verification Company, provides the only solution for true SoC Verification. Utilizing both transactional and 'C' based test strategies in bottom-up and top-down flows, Trek automates testcase generation and results checking for advanced testbenchs. Proven in bottom-up unit level verification and IP reuse efforts Trek also utilizes 'Sparse Models' to verify top-down SoC integrations. Architected to run in your current environment, Trek aggressively verifies complex designs with powerful graphical visualization and analysis of your designs verification space.

Cadence Design Systems, Inc.

San Jose, CA

www.cadence.com

Silver Exhibitor 3
Booth: 2237

Booth: 2012

Booth: 3031

Booth: 1143

Cadence is the global leader in software, hardware, IP, and services that is driving the transformation of the EDA industry. With a focus on EDA360, Cadence embraces the entire spectrum of the design process, improving end-product profitability. This application-driven approach for creating, integrating, and optimizing designs helps customers realize silicon chips, system-on-chip devices, and complete systems at lower costs and with higher quality. The EDA360 approach provides a foundation for innovation, creativity and enhanced productivity in the consumer electronics industry and beyond.

Calypto Design Systems

Santa Clara, CA

www.calvpto.com

Visit booth #2012 to see how Calypto's PowerPro CG (for Clock Gating) and PowerPro MG (for Memory Gating) can automatically reduce power by over 60% in your SoC design. For those of you in the ESL space, Calypto's SLEC product family comprehensively verifies RTL designs generated by the industry's leading highlevel synthesis tools. Calypto empowers SoC and systems designers to develop the highest quality, lowest power electronic systems through its unique power optimization and functional verification tools.



DAC PAVILION Booth #3421

DAC Pavilion brings the technical program to exhibit floor

The DAC Pavilion is the marquee theater on the show floor with over 18 different presentations that address technology and business issues in a fast-paced short presentation format. These 45-60 minute presentations feature the electronic design industries trendsetters and industry insiders. Attendees get the real story on what's real, what's coming and how to be prepared.

Sponsored by:



See pages 52-56 for details



Cambridge Analog Technologies

Billerica, MA

www.cambridgeanalog.com Booth: 2221

Cambridge Analog Technologies, Inc. (CAT) is a provider of leading edge ultra-low power analog circuits including ADC and PLL catering to SoCs built for a wide array of applications such as wireline, wireless, medical, automotive areas, displays, imaging and embedded control. CAT's precision ADC consume 5x-15x lower power relative to competition, and CAT's all-digital integer and fractional-N PLL serve both general purpose and ultra-high performance applications below 1ps jitter. CAT offers world-class support for its clients and partners

Carbon Design Systems

Acton, MA

www.carbondesignsystems.com Booth: 1914, 2127

Carbon Design Systems provides the industry's only unified virtual platformsolution. Carbon's SoCDesigner enables the user to make architecturaldecisions, do performance optimization and validate firmware with 100% accuracyand then automatically generate an equivalent representation which runs at 100sof MIPS to enable application software development. Carbon operates the industry's largest virtual model web portal, delivering 24/7 access to configure, compile, manage and download models from leading IP vendors such as ARM, MIPS, Denali/Cadence, Mentor Graphics and more. Carbon's industry-exclusive model relationships with ARM and MIPS and correspondingunmatched expertise places Carbon at the heart of leading-edge SoC design starts throughout the world.

Carr & Ferrell LLP

Menlo Park, CA

www.carrferrell.com Booth: 3318

Carr & Ferrell LLP is a full-service law firm uniquely positioned to provide strategic patents and intellectual property, corporate, financing and litigation services. Our attorneys leverage their technical, business and legal expertise to help emerging companies and investors transform business concepts into industry leading enterprises.

CAST, Inc.

Woodcliff Lake, NJ

www.cast-inc.com

CAST provides IP cores and platforms for SoC realization, the development of complete systems in FPGAs or ASICs. We feature:

- A competitive processor and microcontroller family, from 8051s through ARM platforms.
- A comprehensive set of image and video processing IP including H.264 and JPEG2000.
- Memory controllers, high-speed interfaces, peripherals, and other IP needed to build complete systems.

Seventeen successful years help us give designers a better IP experience, including proven products, system integration services, and fast, effective support.

Chip Design - Extension Media

San Francisco, CA

www.extensionmedia.com

Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design and Low Power Engineering Portals offer focused editorial content you won't want to miss. And, be sure to visit www.http://eecatalog.com/ for valuable information about all of Extension Media's outstanding technology resources.

Booth: 3024

Booth: 3013

Booth: 1731

Booth: 2517

Chip Path Design Systems

Cupertino, CA

www.chippath.com

Company is the creator of Semantic-IC Design, with tools that define a Cut-and-Paste evaluation methodology for ASIC, FPGA, and ASSP implementation. The ChipRFQ product enables architects to define chips and evaluate Total Cost of Ownership in multiple implementations, with designs distilled into I/O Channels and Subsystems. Each IP contains connectors including AMBA, OCP, and CoreConnect, integrated by Networks-on-Chip (NoC), creating a complete IP Connection Network (IPCN). Company is an information aggregator with an IP Search of 13,000 Semiconductor IPs, 9,000 FPGAs and ASIC analysis in 13 technology nodes. Company's flagship Chip Planner product brings Design Planning (Floorplaning) into the Semiconductor IP age.

ChipEstimate.com

San Jose, CA

www.ChipEstimate.com

All within one site, users can explore an extensive catalog of semiconductor IP and then download the InCyte Chip Estimator tool to predict the die size, power, leakage, performance and cost of their next chip. Visit the ChipEstimate.com booth where you can learn about the latest in semiconductor IP from dozens of IP suppliers on the IP Talks! stage. Join us for hands-on demonstrations and learn how to estimate your next chip's size, power and cost -- in just seconds.

Ciranova, Inc.

Santa Clara, CA

www.ciranova.com

Ciranova is an electronic design automation (EDA) company focused on large productivity improvements in RF, analog and mixed-signal IC physical design. Complementary to existing design flows and supported by leading foundries, Ciranova's PDK and layout automation software dramatically reduces the time and effort needed to implement complex analog functionality in advanced CMOS. Ciranova is a founding member of the Interoperable PDK Libraries (IPL) Alliance and supports the Si2 OpenAccess database. For more information, visit our website at www.ciranova.com.

Booth: 2217

The Network For Advanced IC Designers



Magazines

In-depth coverage of all the technical challenges and implementation options that engineers face in the development and manufacturing of today's complex integrated circuits (IC)

Resource Catalogs

Locate vendors and products including IP, ASIC's, FPGA's, SoC, EDA tools, design services and more





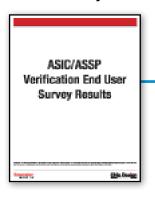
Websites

Online source for the latest tools, technologies and methodologies to better navigate the challenges that face modern IC design environments

Visit *RF and Microwave Systems*Dedicated to covering modeling, design, IP integration and test of RF and microwave functionality into SoCs www.chipdesignmag.com/RFMW

Email Newsletters

Email newsletters and online periodicals with news, commentary and analysis





Market Research

Valuable market intelligence on Chip Design trends

www.chipdesignmag.com

CISC Semiconductor Design+Consulting GmbH

Klagenfurt, Austria

www.cisc.at Booth: 1913

CISC Semiconductor is a design and consulting company for industries developing embedded microelectronic systems with extremely short Time-To-Market cycles. Our competences include system design, simulation, verification and optimization of heterogeneous embedded microelectronic systems. The 3rd generation of CISC tool "System Architect Designer" (SyAD®) is a fully featured simulation based verification environment supporting multi-HDL modeling, automatic test bench generation, black and white box verification, IP-Xact library integration, user access management within an easy to use co-simulation framework for all major simulators.

ClioSoft, Inc.

Fremont, CA

www.cliosoft.com Booth: 1535

ClioSoft is the premier developer of hardware configuration management (HCM) solutions. The company's SOS design data collaboration platform is built from the ground up to handle the requirements of hardware design flows. The SOS platform provides a sophisticated multi-site development environment that enables global team collaboration, design reuse, and efficient management of design data from concept through tape-out. SOS is seamlessly integrated with leading IC design flows - Cadence's Virtuoso® AMS and Custom IC Design, Synopsys' Galaxy Custom Designer, SpringSoft's Laker™ Custom Layout Automation System & Mentor's AMS/Custom IC design.

ClioSoft's Visual Design Diff (VDD) allows engineers to easily identify changes between two versions of a schematic or layout by graphically highlighting the differences directly in the editors.

CLK Design Automation, Inc.

Littleton, MA

www.clkda.com Booth: 1043

CLK Design Automation is the leader in high accuracy timing solutions for nanometer designs. Amber Path FX™ delivers SPICE accurate timing with variance analysis 1,000,000x faster than Monte Carlo SPICE. Amber AOCV Table Generation is the only practical solution for delivering AOCV timing derates in days vs. months for others. With its unique design specific capabilities, Amber FX AOCV tables help designers recapture margin in their existing optimization and timing flows. Amber FX was developed in partnership with TSMC.

CMP

Grenoble Cedex, France

cmp.imag.fr Booth: 2426

CMP is a manufacturing service for ICs and MEMS, for prototyping and low volume production. Integrated circuits are available on CMOS, SiGe BiCMOS, CMOS-Opto from STMicroelectronics and austriamicrosystems, 20 nm FDSOI from CEA-LETI, 3D-IC from TEZZARON/GLOBALFOUNDRIES, 150nm pHEMT GaAs from TRIQUINT and 180nm CMOS power, BCD, CIS from TOWERJAZZ. MEMS are available on various processes: FSBM and MUMPS from MEMSCAP. Design kits for IC CAD tools and Engineering kits for MEMS are available.

CoFluent Design

San Jose, CA

www.cofluentdesign.com Booth: 1815, 2026

CoFluent Design provides Eclipse-based system-level modeling and simulation tools for executing use cases and predicting performance of embedded systems and chips.

CoFluent Studio allows designers to model real-time embedded applications and use cases, simulate their execution on multiprocessor/multicore platforms, and obtain power and performance data.

Models are captured in graphical diagrams using standard UML or CoFluent domain-specific language. Algorithms can be captured in ANSI C/C++ or with MATLAB. Models are translated into TLM SystemC code for host-based simulation.

The generated SystemC can be reused as functional or test model in virtual platform environments.

Booth: 2143

Booth: 1814

Booth: 2416

Concept Engineering GmbH

Freiburg, Germany

www.concept.de

Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers and IC and FPGA designers. Their products include, NIview™ Widgets

- a family of schematic generation engines for EDA tool developers, SpiceVision® PRO
- a customizable debugger for SPICE and DSPF designs, RTLVision® PRO - a graphical debugger for SystemVerilog, Verilog and VHDL designs, GateVision® PRO
- a customizable debugger for Verilog designs. SGvision™ PRO
- · a mixed-mode debugger

Cortus S.A.

Montpellier, France

www.cortus.com

Cortus is the technology leader in ultra low-power, silicon efficient 32-bit microcontroller IP cores. The APS3 combines a power consumption of 22 $\mu\text{W/MHz}$ (130 nm) with up to 1.67 DMIPS/MHz performance. Yet the core itself is no larger than the 8051 – making it the natural upgrade choice for 8-bit/16-bit core users – and is the smallest available core capable of running μCLinux . Microprocessor Report crowned the APS3 the "King of Lilliput". A rich ecosystem of development tools and RTOS are available.

Coupling Wave Solutions

Austin, TX

www.cwseda.com

Coupling Wave Solutions® (CWS) WaveIntegrity platform targets analysis and resolution of parasitic coupling between digital cores and analog or RF blocks and helps successful integration of Mixed-Signal SOCs and SIPs. WaveIntegrity offers full system noise calculations from initial system-level definitions to layout level. WaveIntegrity automatically analyzes the complete system to predict electrical aggression generated by all components, propagation through a combination of interconnects, silicon substrate and package parasitics and the impact on sensitive analog/RF blocks. The technology predicts noise budgets, supports designs having multiple power domains and integrates seamlessly into any customer flows.





ICC, Dresden, Germany March 12-16, 2012

The 15th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications.

The organisation of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results.

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Please visit the DATE website for a list of the topics of interest for DATE 2012.

Submission of Papers

All papers to be submitted electronically by **Sept 11th, 2011** via: http://www.date-conference.com/submit.html
Papers can be submitted either for standard oral presentation or for interactive presentation.

Chairs

General Chair: Wolfgang Rosenstiel, University of Tuebingen, Germany, rosenstiel@informatik.uni-tuebingen.de

Program Chair: Lothar Thiele, ETH Zurich, Switzerland, thiele@tik.ee.ethz.ch

DATE Secretariat - European Conferences, 3 Coates Place, Edinburgh EH3 7AA, United Kingdom **Tel:** +44 131 225 2892 • **Fax:** +44 131 225 2925 • **Email:** sue.menzies@ec.u-net.com

www.date-conference.com

Booth: 1719

Booth: 3120

Booth: 3421

Coventor, Inc.

Cary, NC

www.coventor.com

Coventor is the leading provider of MEMS design automation solutions. Its platform of 3D simulation tools and MEMS expertise significantly reduce the time, cost and effort to optimize performance and bring increasingly complex MEMS devices to market. Coventor's tools combine the capacity and accuracy required for high performance MEMS design and offer an integrated approach to enabling MEMS+IC design. Its solutions are embraced by industry experts who agree that "build and test" is no longer an option as a design platform for MEMS.

CST of America, Inc.

Framingham, MA

www.cst.com Booth: 2516

CST of America, Inc. is the leading supplier of 3D full wave simulation tools worldwide.

CST STUDIO SUITE™ aids in the pre-layout design and post-layout verification of PCBs, packages, interconnects transitions and complete systems. Results such as near and far-end crosstalk, TDR, eye diagrams, SPICE models, electric and magnetic field and current flow are generated and can be optimized. All types of native layout can be imported. CST is a Cadence technology partner and 3D simulation can be run directly from Cadence tools.

Cybereda Corp.

Santa Clara, CA

www.cybereda.com

Discover the ADDS software suite for the fast detection, and repair of bugs in transistor circuits for analog, mixed-signal and digital designs. The suite features the ADDS-Debugger, with its extensive signal-tracing, analysis, and reporting capabilities, the PCSim true-SPICE parallel simulator, and a new waveform viewer and calculator, ADDSWave. The Cybereda suite delivers a 10X breakthrough in designer productivity by automating and accelerating the debug analysis process. With the ADDS suite, the right answers can be had in hours not days.

DAC Pavilion

Louisville, CO

www.dac.com

The DAC Pavilion, Sponsored by GLOBALFOUNDRIES, brings the technical conference to the exhibit floor with a wide variety of panels and presentations featuring twenty technical, business and strategy discussions. Panels include discussions on 3-D ICs, embedded system design, multi-core, low-power design, Analog PDKs, IP, Synthesis and Verification. In addition, the Pavilion offers sessions on Android, Meego and Linux, "Teen Talk" on electronics, and the popular Gary Smith on EDA trends and Jim Hogan on the semi ecosystem. See pages 52-56, visit DAC.com or stop by the Pavilion booth 3421 for a complete schedule. Presentations are free for all attendees.

Dassault Systemes Americas Corp.

Lowell, MA

www.3ds.com

A world leader in 3D and Product Lifecycle Management (PLM) software and services, Dassault Systèmes (DS) brings value to 115,000 customers in 80 countries. The DS portfolio includes CATIA for virtual design, SolidWorks for 3D mechanical design, DELMIA for virtual production, SIMULIA for virtual testing, ENOVIA for global collaboration and 3DVIA for online 3D experiences.

Booth: 1625

Booth: 1915

Booth: 3316

The ENOVIA Synchronicity DesignSync solutions uniquely address a rapidly emerging use for PLM by helping customers connect their electronic design environments directly to the extended enterprise. This enables globally dispersed design teams to collaborate in real time, reducing design and development costs, leveraging design expertise, improving quality and accelerating time to market. Learn more at http://www.3ds.com/enovia/semiconductor

DATE 2012

Edinburgh, United Kingdom

www.date-conference.com Booth: 2630

DATE is the complete event for the European electronic system and test community. A world-leading conference and exhibition, DATE unites 2300 professionals with some 60 exhibiting companies, cutting-edge R & D, industrial designers and technical managers from around the world. As per previous editions the DATE 2012 conference will feature two special days. The technical paper submission is 11 September 2011. Please visit our website for further details.

Design and Reuse

Grenoble, France

www.design-reuse.com

Founded in 97, D&R became the worldwide leader as a web and a B2B portal in the IP/SoC field with its 70,000 Absolute Unique Visitors / Month (source: Google Analytics), 15,000 daily updated IP/SOC products descriptions, its News broadcast to 35,000 subscribers... Based on 13 years experience, D&R sells a Java/XML multi application, configurable enterprise platform offering the most innovative and straightforward solution for your hottest needs such as Web Product cataloguing, intranet Design Reuse Platform, External suppliers management...

Dini Group

La Jolla, CA

www.dinigroup.com

Products featuring Xilinx Virtex-6 technology will be on display, including the new DN2076k10 with 6 LX760 devices. Dini will also display the world's largest ASIC Prototyping Platform, the DN7020k10 with 20 Altera Stratix-4 devices providing more than 130 million ASIC gates.

Founded in 1995, the Dini Group has supplied over 5 billion ASIC gates and driven prices below 1/4 Cent/ASIC gate.



At Dassault Systèmes, Innovation is a Core Value

Innovation is at the core of successful Semiconductor and High-Tech Electronics companies. Understanding how to incorporate new, innovative technologies into the next 'must have' products customers are demanding – and validate those products without delaying rapid launch schedules is critical.

Semiconductor and High-Tech Electronics companies need effective solutions to:

- rapidly evaluate design performance
- foster collaboration across multiple design teams
- access latest data on product parts and IP
- leverage the know-how of experts using advanced EDA tools
- ensure compliancy with rigid government regulations

That's why, to stay competitive, more than 25 leading global consumer electronics manufacturers and more than 100 semiconductor organizations, including 17

of the top 20, are using solutions from Dassault Systèmes, including **ENOVIA Synchronicity**, for collaborative design management and **SIMULIA Abaqus FEA** software for realistic simulation.

Advanced PLM (Product Life Cycle Management) solutions from Dassault Systèmes (DS) enable companies to manage change and streamline their processes more effectively – from idea generation to concept validation, including product portfolio management visibility, collaborative IP development, sourcing, production, change management and sign-off.

Visit DS at Booth #1625 in Hall F to meet with DS experts, view a live demo or experience some "3D" fun...and enter for your chance to win an iPad!

To set up a meeting on-site with our DS High-Tech Electronics and Semiconductor experts to learn more about our technology, please contact Jim Webb at: james.webb@3ds.com or (978) 442-2605.



Booth: 3139

Booth: 3114

Booth: 2931

DOCEA Power

Moirans, France

www.doceapower.com Booth: 1912

DOCEA Power develops and commercializes a new generation of methodology and ESL tools for enabling faster and more reliable power and thermal modelling at system level. DOCEA Solution based on the ACEplorer® platform is a consistent approach for executing architecture exploration and optimizing power and thermal behaviour of electronic systems at an early stage of the project.

Dorado Design Automation, Inc.

San Jose, CA

www.dorado-da.com

Dorado expands the scope of ECO to be "All the incremental jobs to be done in the ECO phase", and commit to provide solutions for all ECO issues. Dorado's Tweaker family covers all possible incremental jobs such as Functional ECO, Timing ECO, Metal ECO, Power ECO, and the interesting pre-route ECO for SI prevention. Tweaker family is developed with ECO specific architecture and algorithm. It supports 40nm and below.

Doulos

San Jose, CA

www.doulos.com

Doulos is the global leader for the development and delivery of world class training solutions in electronics engineering.

Fully independent, Doulos sets the industry standard for the highest quality training programs, covering the needs of hardware designers, embedded software developers and system design and verification specialists implementing complex SoC and FPGA designs.

The natural partner for leading tool and technology companies, Doulos schedules classes across the U.S. and Europe and delivers in-house training programs world-wide. For more information, visit http://www.doulos.com.

Duolog Technologies Ltd.

Sandyford - Dublin, Ireland

www.duolog.com

Duolog introduces Socrates – the hub for IP integration. Socrates replaces ad-hoc scripted solutions with a centralized, standardized, synchronized IP integration platform. The Socrates tools incorporate IP packaging, register management, rules-based system assembly and I/O fabric creation. Socrates auto-generates multiple design views from a standardized, centralized data source so that all teams are synchronized at all times, guaranteeing higher quality designs, more predictable schedules and fewer bugs. The Socrates tools fully support IP-XACT and run on Windows or Linux platforms.

E-System Design

Johns Creek, GA

www.e-systemdesign.com

E-System Design was founded in March 2009 by industry leading EDA, Semiconductor, and Signal and Power Integrity experts to provide EDA software focused on enabling System Integrity through Signal and Power Co-simulation of complex, high speed and highly integrated IC packages, SIPs, printed circuit boards, and systems. E-System Design's initial product, "Sphinx" is a "Best in Class" Signal and Power Co-simulator capable of accurately simulating critical paths through complete designs for evaluation and signoff of new designs for production release.

Booth: 3121

Booth: 2825

Booth: 2118

Booth: 1221

EDA Cafe-IB Systems

Campbell, CA

www.edacafe.com

Thousands of IC, and system designers visit EDACafé.com to learn about the latest company news and research the latest design tools and services. As the #1 EDA portal it attracts more than 75,000 unique visitors each month and leverages TechJobsCafe.com to bring you targeted job opportunities. EDACafé reaches out to more than 30,000+ EDA professionals with its daily CaféNews. EDACafe will be doing video interviews of industry executives at its DAC booth. Please visit to hear all the conference buzz.

EDXACT SA

Voiron, France

www.edxact.com

EDXACT provides technology helping layout designers to speed up the verification of design, taking parasitic effects into account. At 110nm and below, the netlist parasitics substantially slow down established simulation tools. EDXACT speeds up flow performance without major retooling and provides new solutions for quick analysis. The tools are used in production every day at more than 30 sites all over the world by the leading semiconductor companies, IDM and fabless. Main tools are JIVARO for standalone netlist reduction and COMANCHE for fast and accurate comparative layout analysis.

element 14

Chicago, IL

www.element14.com

Launched in June 2009, element14 is the first online collaborative community, information portal and electronics store. It offers design engineers extensive product data, the latest technology products, and innovative tools and services to reduce design cycle time, increase productivity and speed time to market. The website's newest innovation will be revealed at DAC at the element14 booth. element14 (www.element14.com) is an offering from Premier Farnell, a global leader in multi-channel electronics distribution, trading in North America as Newark.

TechJobsCafé PCBCafé Tutorials

Videos

EDACafé News Blogs IP Catalog

As the #1 EDA portal, EDACafe.com attracts more than 75,000 unique visitors each month and leverages TechJobsCafe.com to bring you targeted job opportunities. EDACafé reaches out to more than 30,000+ EDA professionals with its daily newsletter. Sign up for our daily newsletter at EDACafe.com.

www.EDACafe.com

Booth: 3324

Booth: 2836

Embedded Theater

Louisville, CO

www.dac.com Booth: 1825

The ESS Zone is a special area on the DAC exhibit floor dedicated to displaying products and services from embedded systems and software vendors. Visit the Embedded Theater in booth 1825 to see Tear-Down presentations by iSupply, technical presentations from all Embedded System and Software Zone exhibitors, and IP presentations brought to you by the IP/SoC booth participants. Check the DAC website for a complete schedule of presentations. Presentations are free for all attendees.

Entasys Inc.

Seoul, South Korea

www.entasys.com

Entasys is a leading provider of Electronic System Level(ESL) Silicon Virtual Prototyping(SVP) solutions. Feasibility analysis with SVP solution allows designers to predict the design problems of IC implementation and to reduce design time by over 30% for RTL hand-off.

Pillar-DP-Optima is an optimal pad configuration tool to optimize the number and location of power/ground pad in the peripheral IO and flip chip design. Pillar-DP-Navis is an industry-proven SVP solution including routing congestion analysis and interconnect delay estimation of RTL/pre-RTL floorplanning

EUROPRACTICE

Leuven, Belgium

www.imec.be Booth: 3027

The EUROPRACTICE IC Service (IMEC and Fraunhofer) offers low cost ASIC prototyping and small volume fabrication. Low cost prototyping is offered through regularly scheduled Multi Project Wafer runs, whereby several designs are merged onto the same fabrication run,fabricated in CMOS, BiCMOS and SiGe processes from 0.8um to 40nm at ON Semiconductor, austriamicrosystems, IHP, LFoundry, TSMC and UMC. A total design and manufacturing flow is offered including cell library and design kit support, RTL-to-layout, prototyping, volume fabrication, assembly and test.

EVE-USA, Inc.

San Jose, CA

www.eve-team.com

EVE's ZeBu hardware-assisted verification platforms, including its 7 th generation ZeBu-Blade, provide industry leading HW-SW Coverification solutions offering the highest performance and lowest cost-of-ownership in emulation.

Hardware designers and embedded software developers can slash the time and cost of complex SOC development, leveraging ZeBu across the entire design cycle.

ZeBu provides flexible multi-mode emulation, interfacing with Verilog, SystemVerilog and VHDL-based simulators, Electronic-System Level (ESL) tools, and target hardware systems across the range of computer, consumer, networking, communications, and automotive industries.

Exhibitor Forum

Louisville, CO

www.dac.com

The Exhibitor Forum provides a theater on the exhibit floor where exhibitors present focused, practical technical content to attendees. Each session is devoted entirely to a specific domain (e.g., verification or system-level design) and consists of presentations from two to three companies. The Exhibitor Forum provides exhibitors and attendees with a great way to network, and learn practical "how-to" information on new technologies.

Booth: 1005

Booth: 1813

Booth: 2939

Booth: 1304

ExpertIO, Inc.

www.expertio.com

ExpertIO, Inc. is a world-class provider of Verification IP. Our goal is to deliver the highest quality and easiest to use Verification IP on the market. Founded in 2002, ExpertIO has been entrusted by clients around the world when time to market matters.

Current Verification IP products include:

- PCI Express G1-3
- Ethernet (10Mb to 100Gb)
- SAS
- SATA
- Fibre Channel

Our products are designed and backed by our all senior engineering team of protocol verification experts. ExpertIO also offers DV Services. Let ExpertIO help you achieve 1st pass success and improve your time to market!

Phone: 408-217-1901

Extreme DA

Santa Clara, CA

www.extreme-da.com

Extreme DA delivers the fastest path to Timing Closure and Signoff. Discover how ECO loops can run 10X faster with the new generation GoldCap parasitic extractor, and the proven GoldTime analyzer which delivers the fastest runtimes and 500M gate capacity. Learn how GoldTime POCV delivered customer success, is faster and less pessimistic than AOCV, and why top fabless companies have adopted GoldTime. Whether verifying timing at 65nm or yield at 28nm, Extreme DA delivers the right answers you need – FAST!"

FishTail Design Automation, Inc.

Lake Oswego, OR

www.fishtail-da.com

FishTail Design Automation offers a unique approach to improving chip implementation by automatically generating, merging, promoting and verifying golden timing constraints early in the design cycle. FishTail's products allow designers to drive chip-implementation with complete constraints that are formally proven to be correct and to then manage these constraints as chip-implementation progresses. The result is a shorter chip-implementation schedule with much fewer back-end timing closure iterations. Also, by formally proving the correctness of design constraints you eliminate the risk of silicon failure resulting from incorrect timing exceptions.



EXHIBITOR FORUM



Booth: 2725

Forte Design Systems

San Jose, CA

www.forteds.com Booth: 3417

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction and improve design results. Its innovative synthesis technologies and intellectual property offerings allow design teams creating complex electronic chips and systems to reduce their overall design and verification time. More than half of the top 20 worldwide semiconductor companies use Forte's products in production today for ASIC, SoC and FPGA design. Forte is headquartered in San Jose, Calif., with additional offices in England, Japan, Korea and the United States. For more information, visit www.forteds.com.

GateRocket, Inc.

Bedford, MA

www.gaterocket.com Booth: 3126

GateRocket addresses the increasing challenge of verifying and debugging complex FPGAs. Its unique Device Native® approach verifies the design using the targeted FPGA device in its RocketDrive® verification system, saving weeks in the debug lab, eliminating costly synthesis-place-route iterations, and reducing FPGA bring-up time by 50% or more. The RocketDrive and its accompanying software debug tool, RocketVision®, turn an existing HDL simulator into a powerful and efficient FPGA debugging system that reduces the 'vicious cycles' of traditional FPGA design approaches.

GIDEL

Santa Clara, CA

www.gidel.com

GiDEL, the first company to provide third-generation ASIC Prototyping systems in the market, will be showcasing its new generation of the PROCSoC Verification System. The PROCSoC family is designed to debug and verify SoC designs of diverse design styles. The new generation has quadrupled the capacity of the system by incorporating Altera's new Stratix IV 820E, the world's largest and fastest 40nm FPGA available today. The PROCSoC system incorporates advanced software tools, enabling easy HW/SW co-development and powerful debug features, and is packaged in two types of chassis each providing a high degree of flexibility and mobility. For more information, contact GiDEL in North America at 408-969-0389, or on the web at www.gidel.com

GLOBALFOUNDRIES

Milpitas, CA

www.globalfoundries.com

GLOBALFOUNDRIES is the World's first full-service semiconductor foundry with a truly global manufacturing and technology footprint. Launched in March 2009 through a partnership between AMD [NYSE: AMD] and the Advanced Technology Investment Company (ATIC), GLOBALFOUNDRIES provides a unique combination of advanced technology, manufacturing excellence and global operations. With the integration of Chartered Semiconductor in January 2010, GLOBALFOUNDRIES significantly expanded its capacity and ability to provide best-in-class foundry services from mainstream to the leading edge at 65nm, 45nm, 28nm and 20nm.

Platinum Exhibitor

Booth: 1517

Booth: 1517

Booth: 1517

Booth: 1517

GLOBALFOUNDRIES Partner - Analog Bits

Mountain View. CA

www.analogbits.com

Analog Bits, Inc. is the leading supplier of integrated timing and interconnect IP. Products include precision clocking macros such as PLL's & DLL's, programmable interconnects such as multi-protocol SERDES/PMA and programmable I/O's as well as specialized memories such as high-speed SRAMs and T-CAMs. With billions IP fabricated in customer silicon from 0.35-micron to 28-nanometer processes, Analog Bits has the heritage of "first time working silicon" at merchant foundries and IDMs. For more information visit www.analogbits.com

GLOBALFOUNDRIES Partner - Apache Design

San Jose, CA

www.apache-da.com

Apache Design Solutions, Inc. is a leading provider of innovative power analysis and optimization solutions that enable the design of power-efficient, high-performance, noise-immune ICs and electronic systems. Apache's comprehensive suite of integrated products and methodologies advances low-power innovation and provides a competitive advantage for the world's top semiconductor companies to help lower power consumption, increase operating performance, reduce system cost, mitigate design risks, and shorten time-to-market for a broad range of end-markets and applications.

GLOBALFOUNDRIES Partner - Cadence

San Jose, CA

www.cadence.com

Cadence is the global leader in software, hardware, IP, and services that is driving the transformation of the EDA industry. With a focus on EDA360, Cadence embraces the entire spectrum of the design process, improving end-product profitability. This application-driven approach for creating, integrating, and optimizing designs helps customers realize silicon chips, system-on-chip devices, and complete systems at lower costs and with higher quality. The EDA360 approach provides a foundation for innovation, creativity and enhanced productivity in the consumer electronics industry and beyond.

GLOBALFOUNDRIES Partner - ChipEstimate.com

San Jose, CA

www.ChipEstimate.com Booth: 1517

All within one site, users can explore an extensive catalog of semiconductor IP and then download the InCyte Chip Estimator tool to predict the die size, power, leakage, performance and cost of their next chip. Visit the ChipEstimate.com booth where you can learn about the latest in semiconductor IP from dozens of IP suppliers on the IP Talks! stage. Join us for hands-on demonstrations and learn how to estimate your next chip's size, power and cost -- in just seconds.

GLOBALFOUNDRIES Partner - Lorentz Solution

Santa Clara, CA

www.lorentzsolution.com Booth: 1517

Lorentz Solution supplies EDA products focused on costsensitive RF and high-speed semiconductors at advanced process nodes. The PeakView™ EM Design Platform provides silicon predictability through high-accuracy EM-based synthesis, extraction and modeling. Integrated with industry standard EDA design and PDK platforms, PeakView removes barriers letting chip designers perform their own EM device design and circuit level EM verification for predictable circuit performance and reduced chip area.

GLOBALFOUNDRIES Partner - Mentor Graphics

Wilsonville, OR

www.mentor.com Booth: 1517

Mentor Graphics is a world leader in EDA products for electronics and semiconductor companies. Mentor offers solutions that meet the demand for short design cycle time, improved productivity, and high yield, including tools for electronics system level design and simulation, embedded hardware/software co-development, system and IC verification, IC physical design and verification, testing and yield enhancement. Products include the Olympus-SoC place and route system, the Calibre PV and DFM platform, and the Tessent suite for comprehensive IC test, failure diagnosis and accelerated yield learning.

GLOBALFOUNDRIES Partner - Synopsys

Mountain View, CA

www.synopsys.com Booth: 1517

Fast Forward to Predictable Success with the EDA software, intellectual property (IP) and services needed to meet today's ever increasing time-to-market semiconductor design and manufacturing demands. With the explosion of "smart" consumer devices driving design needs, Synopsys' comprehensive portfolio of integrated system-level, implementation, verification, IP, manufacturing, and design flow solutions optimized for GLOBALFOUNDRIES' technologies can help designers address their key design and manufacturing challenges. Visit Synopsys to learn more about how to put your next design targeted to GLOBALFOUNDRIES silicon on fast forward to predictable success.

GLOBALFOUNDRIES Partner - Toppan Group

Tokyo, Japan

www.photomask.com

Toppan Electronics is a premier supplier to the electronics industry, providing a wide range of products, including Photomasks. Our photomask business uses a global network of production sites and data centers supporting our global customer base. We produce a full range of photomask products, for multiple end use applications, at design rules (starting at 20nm) and in formats to support a wide variety of image transfer applications.

Booth: 1517

Booth: 3249

Gradient Design Automation

Santa Clara, CA

www.gradient-da.com

What if you knew the temperature profile inside your chip before tapeout? High performance chips have areas with very high power density, causing temperature to rise unevenly within the die. Gradient's HeatWave™ thermal simulator produces a full-chip, three-dimensional temperature profile at device- and interconnect-level resolution. Instance-specific temperatures are annotated into your netlist, giving you thermally-accurate electrical analysis. The designer can pinpoint hotspots and excessive temperature variations and avoid thermally-induced circuit failures, performance degradations, and reliability issues before building the chip.

GRID Simulation Technology, Inc.

Morgan Hill, CA

www.gridsimtech.com Booth: 1918

GRID Simulation Technology, Inc. is a Silicon Valley-based Electronic Design Automation (EDA) company dedicated to solving the world's largest and most complex electronics problems at true SPICE-accuracy through its revolutionary new analysis technology. The company's flagship products, NanoRAIL™ and SimCHECK™, provide analysis of IC power grid problems including IR voltage drop and electro-migration (EM), and the qualification of complex power network analysis results. The company is a privately held California Corporation headquartered in Morgan Hill, CA and with offices located in: East Fishkill, NY; and Tokyo, Japan.

Helic, Inc.

San Francisco, CA

www.helic.com Booth: 3049

Helic provides Electronic Design Automation (EDA) software tools and semiconductor intellectually property (IP), with a mission to enable increased levels of miniaturization for semiconductor-based wireless and broadband systems.

We are a world leading provider of rapid electromagnetics modeling and RF silicon synthesis and verification technologies. In more than a decade of service to leading semiconductor companies, we are revolutionizing the way ICs and modules are being designed, verified and manufactured.



MANAGEMENT DAY

TUESDAY, JUNE 7

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SEE PAGE 12 FOR DETAILS



ESS EXECUTIVE DAY

WEDNESDAY, JUNE 8

EMBEDDED SYSTEMS AND SOFTWARE

MEETS

HARDWARE

SEE PAGE 13 FOR DETAILS

Booth: 1617

Hewlett-Packard Co.

Cupertino, CA

www.hp.com Booth: 2730

HP, the leader in High Performance Computing, delivers Converged Infrastructure solutions that maximize product innovation, minimize time-to-market and development costs, while adapting quickly to change. Converged Infrastructure solutions are well adapted to demanding EDA workloads — workstations, servers, storage, networking, power and cooling and software, supported through close relationships with EDA software vendors. The World's largest technology company, HP brings together a portfolio that spans printing, personal computing, software, services and IT infrastructure to solve customer problems.

IBM Corp.

Armonk, NY

www.ibm.com Booth: 1818

IBM Rational provides a collaborative life-cycle approach to codevelopment of hardware and software for building the next generation of innovative products. As the leader in custom logic for the communications infrastructure and analog & mixed-signal specialty foundry technology manufacturing, IBM's silicon powers the World's most innovative products to enable a Smarter Planet.

IC Manage, Inc.

Los Gatos, CA

www.icmanage.com

The IC Manage Global Design Platform (GDP) lets designers track, control, and distribute design, configuration, and IP property data. It enables swift and accurate derivations from existing IP, empowering your team to reuse existing assets.

IC Manage GDP stores and maintains your global organization's design, stimulus, results, bug tracking and documentation data spanning digital and custom flows - in one common place. All data that is authorized for sharing is rapidly accessible worldwide and secured by IC Manage ArmorT protection.

Imera Systems, Inc.

San Jose, CA

www.imera.com Booth: 3225

Imera Systems provides an on-demand, unified secure network infrastructure to connect and protect enterprises in the semiconductor ecosystem. Imera virtual security solution enables elastic protection for data and applications hosted in cloud environments to meet corporate and regulatory compliance. Imera virtual application network solution offers secure access to resources protected in cloud environments and enables federated collaboration across ecosystem partners. Imera solutions help enterprises to maximize productivity, minimize security risks, and ensure total IT and business agility.

Infotech Enterprises

San Jose, CA

www.infotech-enterprises.com

Infotech Enterprises has over 8,000 employees in 30 worldwide locations. We provide engineering services for RTL Design & Verification, DFT, Synthesis/Timing, Physical Design & Verification, Custom/Analog Layout, Embedded Software (board support package, middleware customization, OS porting, device driver development, connectivity software development and multimedia component (audio/video) integration) and FPGA/Board design with 12 year impeccable track record of "first pass success" on over 200 design projects across various nodes up to 40nm.

Booth: 2716

Booth: 1715

Booth: 3216

Booth: 2220

InnoPower Technology Corp.

Sunnyvale, CA

www.innopower-tech.com

Innopower - world leading semiconductor IP provider with experienced engineering teams in supporting very high-volume production. These IP products are highly differentiated and are in use by many fabless design companies. The product offering focuses on the fundamental libraries (standard cells, memory compilers and I/O's) which are feature-rich and innovative. In addition, the broad product portfolio includes other IP's, such as special I/O and standard interface IPs. With the breath of its offering and competitive specifications, Innopower is there to support any SOC designs, whether the application is in consumer electronics, computer or communication.

InPA Systems, Inc.

San Jose, CA

www.inpasystems.com

InPA Systems is an emerging EDA start-up that focuses on making multi-FPGA prototyping much more productive. Today's FPGA prototypes are indispensible for SoC verification and validation but are difficult to use due to low visibility, frequent iterations of FPGA P&R, and a lack of verification methodology. InPA Systems introduces technology that provides full signal visibility inside the FPGA, a unique programmatical method for reducing the number of FPGA P&R cycles, coupled with a zoom in/out methodology for debugging software and hardware in today's SoCs.

Interra Systems, Inc.

Cupertino, CA

www.interrasystems.com

Interra Systems provides Design Automation technologies and services. Automation technologies from Interra include MC2, a Memory Development System and EDA Objects, standards-compliant EDA front-ends. EDA Objects include SystemVerilog, Verilog, VHDL and several other EDA language parsers, elaborator and synthesis engine. MC2 is a platform for memory designers for memory architecture definition, characterization and compiler creation.

Interra design services include methodology automation, tools integration and memory design and characterization. Interra's Design automation Solutions are backed by deep EDA solutions expertise. http://www.interrasystems.com/eda/



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Fully integrated learning packages meticulously researched by leading subject matter experts. They enable serious computing professionals to gain an in-depth understanding of specific fields. Current offerings include Cloud Computing and Parallel Computing, with Mobility, Security, Software as a Service (Saa S) and more to come. http://techpack.acm.org

ACM Learning Center

ACM members can now access additional advanced technology courses through the ACM Learning Center **Element K** portal. Notably, the latest courseware in ACM's custom collection features content from premier training providers **Sun** and **Microsoft**. http://learning.acm.org

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The ACM Online Books program includes **full access to 600 online books** from Safari® Books Online (professional members only), and **500 online books** from Books24x7®. We've expanded our online book offerings to include even more timely and popular selections from O'Reilly and other leading publishers, now including videos.

The ACM online course program features **full access to over 3,800 online course titles** in multiple languages and 1,100+ virtual labs. These courses are open to ACM Professional and Student Members on a wide range of technical and business subjects. **http://learning.acm.org**

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www.acm.org/chapters

ACM Publications
www.acm.org/publications

ACM Advanced Member Grades
http://awards.acm.org

ACM-W http://women.acm.org

ACM Electronic Services

https://www.myacm.org/dashboard.cfm

Booth: 1931

Booth: 2317

Booth: 1924

Isilon Systems

Seattle, WA

www.isilon.com Booth: 3213

Isilon, a division of EMC, is the global leader in scale-out storage. We deliver powerful yet simple solutions for enterprises that want to manage their data, not their storage. Isilon's products are simple to install, manage and scale, at any size. And, unlike traditional enterprise storage, Isilon stays simple no matter how much storage is added, how much performance is required or how business needs change in the future.

Jasper Design Automation, Inc.

Mountain View, CA

www.jasper-da.com

Jasper Design Automation offers innovative solutions, based on formal technologies, for the design and verification of semiconductor IP and SoC. Jasper delivers advanced formal technology, software and services to customers in the global IC markets including consumer, wireless, computing, network, graphics, and more. Flagship products JasperGold, ActiveProp, ActiveDesign, and JasperCore provide customers with a competitive advantage by delivering targeted ROI throughout the design cycle. Headquartered in Mountain View, California, Jasper is privately held and has offices and distributors worldwide. Upgrade your verification with Jasper: http://jasper-da.com.

JTAG Technologies

Easton, MD

www.jtaglive.com

JTAG Live, the easy-to-use and extremely economic board debug tool, comes from JTAG Technologies. We've been in the boundary-scan business since 1993, and we've used that experience to create an all-new, low-cost tools suite accessible to every engineer and technician involved in PCB debug and test. As hardware designers ourselves, we know the pressures facing today's EE. Design a new product that's highly functional and meets strict cost and reliability objectives. And, of course, be sure to get your prototypes up and running quickly. Underneath the skin of JTAG Live is the power of boundary-scan, capitalizing on the built-in test resources in many of the chips on your board. But to use JTAG Live, you don't need to know the anything about boundary-scan, because we did that part for you.

Laflin/Instigate

Portland, OR

www.laflinltd.com

Laflin Limited sells/supports EDA tools, IP, and Design Services for leading providers in the electronics industry. Represented at DAC will be: Instigate Design, a design services company based in Armenia, with more than 50 successful customer engagements in U.S./Europe and a staff of ~100 engineers. Expertise lies in virtual prototyping, parallel programming, embedded S/W and OS development, system-level & software design and verification. HOTSCOPE v7.6.2 from JEDAT(/DNP) will be on display with its enhanced equivalent net trace capability, schematic viewing of SPICE and EDIF netlists, and LEFDEF net connectivity and element viewing.

Library Technologies, Inc.

Saratoga, CA

www.libtech.com

Exhibiting ChipTimer, design reoptimization and power and timing closure tool. It improves clock speed by ~30-100%, reduces area by ~10-30% and leakage power by several factors, Using design-specific library cells derived from existing library as necessary, works for all processes, in both pre-/postlayout flows. Come to see SolutionWare for library creation of all flavors, standard cell, IO and memory, and CellOpt circuit optimizer for standard cells which reduces power dissipation while meeting cell specs, and YieldOpt for managing process variation.

Magma Design Automation, Inc.

San Jose, CA

Gold Exhibitor

Booth: 1743

Booth: 2417

Booth: 1135

www.magma-da.com

Magma is redefining SoC, ASIC, analog/mixed-signal, memory and high-performance core design with truly integrated digital and analog IC implementation. Visit us to learn how Magma technology handles 10-million-cell digital designs flat, how analog design is automated and IP reused, and how multi-scenario timing analysis can be done on a single-CPU machine. You'll also see that virtually any design can be physically verified in a few hours, SPICE-accurate simulation can be done 10X faster, and an order-of-magnitude improvement in library characterization throughput can be achieved.

Magwel NV

San Jose, CA

www.magwel.com

Magwel's Power Transistor Modeler simulates large power transistor arrays, ESD and power distribution networks to extract 3D resistance, analyze electro-migration problems, IR drops, and electro-thermal hotspots with 3D accuracy and unprecedented speed. Substrate Noise Analyzer models substrate noise injection (minority and majority carriers), propagation and coupling in large critical layouts. DevEM co-simulates semiconductor active and passive devices together with metal stack. Parasitic Extraction Tool extracts R, L and C on large critical nets.

Mentor Embedded

Wilsonville, OR

www.mentor.com Booth: 1718,1720, 1819,1821

Mentor® Embedded, the Mentor Graphics family of comprehensive embedded products and services, enables users to build, debug, profile, and analyze advanced embedded systems. The Mentor Embedded portfolio includes open source development tools, software and middleware, sophisticated 2D/3D UI development, JTAG probes, target hardware, and professional services to create all-inclusive and highly integrated design solutions. With Mentor Graphics, developers and silicon partners alike can optimize their products for improved performance and cost efficiency without being confined by proprietary IP. Visit www.mentor.com/embedded.



EMBEDDED SYSTEMS AND SOFTWARE (ESS) ZONE



Booth #1825

DAC is bringing together Embedded Systems and Software (ESS) vendors in the new ESS Zone to showcase embedded systems tools, IP, and services. In parallel with the major increase in embedded systems and software research and technical presentations offered at DAC, ESS Zone exhibitors will be presenting their embedded solutions in the ESS Zone theatre. Other high profile talks and presentations are scheduled as well.

Booth: 1821

Booth: 1718

Booth: 1720

Booth: 1819

Mentor Embedded / Freescale Semiconductor

Wilsonville, OR

www.freescale.com

Freescale Semiconductor is a global leader in the design and manufacture of embedded semiconductors for the automotive, consumer, industrial and networking markets. The privately held company is based in Austin, Texas, and has design, research and development, manufacturing and sales operations around the world. Visit http://www.freescale.com.

Mentor Embedded / MIPS Technologies, Inc.

Wilsonville, OR

www.mips.com

MIPS Technologies is a leading provider of industry-standard processor architectures and cores that power some of the world's most popular products for the home entertainment, communications, networking and mobile device markets. These include Linksys broadband devices; Sony DTVs and digital consumer devices; Pioneer DVD recordable devices; Motorola digital set-top boxes; Cisco network routers; and Hewlett-Packard laser printers. Founded in 1998, MIPS Technologies is headquartered in Sunnyvale, California, with offices worldwide. Visit the website: www.mips.com.

Mentor Embedded / NetLogic Microsystems

Wilsonville, OR

www.netlogicmicro.com

NetLogic Microsystems is a worldwide leader in high-performance intelligent semiconductor solutions that are powering next-generation Internet networks. NetLogic Microsystems' best-inclass products perform highly differentiated tasks of accelerating complex network traffic to significantly enhance the performance and functionality of advanced 3G/4G mobile wireless infrastructure, data center, enterprise, metro Ethernet, edge and core infrastructure networks. NetLogic Microsystems is headquartered in Santa Clara, California, with offices and design centers throughout North America, Asia and Europe. Visit www.netlogicmicro.com.

Mentor Embedded / Texas Instruments

Wilsonville, OR

www.ti.com

Texas Instruments semiconductor innovations help 80,000 customers unlock the possibilities of the world as it could be – smarter, safer, greener, healthier and more fun. Our commitment to building a better future is ingrained in everything we do – from the responsible manufacturing of our semiconductors, to caring for our employees, to giving back inside our communities. This is just the beginning of our story. Learn more at www.ti.com.

Mentor Graphics Corp.

Wilsonville, OR

www.mentor.com

Mentor Graphics is a technology leader in electronic design automation, providing software and hardware design solutions focused on electronic design and physical verification, functional verification, FPGA/PLD, design-for-test, PCB design, embedded software and thermal analysis. Our innovative tools help designers solve current and future design challenges such as scalable solutions for functional verification including emulation; cutting edge technology for design-for-manufacturability and mixed-level IC design verification; award-winning test compression technology; embedded software development systems; and market-leading integrated system design solutions.

Platinum Exhibitor

Booth: 1542

Booth: 2921

Booth: 2917

Methodics LLC

San Francisco, CA

www.methodics-da.com

"Methodics LLC is a leading provider of data management (DM) systems for IC Design. The ProjectIC IP Assembly and Reuse Platform manages and delivers IP to SOC project teams across remote design sites. User workspace configuration is managed by Bills of Materials and project IP activity is tracked in a scalable database. ProjectIC supports Subversion, Perforce, ClearCase and Git configuration management systems and in conjunction with the VersIC Subversion/Perforce integration to Cadence provides a best-in-class solution to the problem of DM across large SOC designs".

Micro Magic, Inc.

Sunnyvale, CA

www.micromagic.com

Micro Magic, Inc. - Chip Solutions Company MMI provides tools and services for high-speed, low-power Systems on Chip. MMI Tools are field proven with hundreds of tapeouts over ten years. DataPath Compiler - DPC - a unique solution for optimizing datapaths for high-speed and low-power. New DPC features include Verilog-only and gate Auto-sizing. MAX-3D - the only layout tool for 3D TSV designs. MMI design services provide a plug-and-play solution. You need us if you absolutely, positively must make timing!

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www.InsideChips.com

Mirabilis Design Inc.

Sunnyvale, CA

www.mirabilisdesign.com Booth: 2219

Mirabilis Design provides model-based design of SoC and electronics systems for performance optimization, power measurement, and software user-case validation. Using dynamic simulation and graphical model entry, designers can quickly assemble models of their proposed systems using pre-built components, and simulate with workloads and fault injection scenarios. The pre-built reports can be extensively analyzed to make product specification decisions. Demonstrations will cover SoC (Buses, Memories and Processors), Automotive (AUTOSAR and Ethernet), and Aerospace (ARINC 653 and Avionics).

Mixel, Inc.

San Jose, CA

www.mixel.com Booth: 3127

Mixel is a leading provider of differentiated mixed-signal IP cores to the semiconductor and electronics industries, with a particular focus on low power mobile applications. Our silicon-proven IP cores utilize a LegorithmicTM approach and are highly configurable for a wide range of applications. This enables our customers to develop new systems rapidly, reducing risk, time-to-market, and development and manufacturing costs. For more information, please visit: www.mixel.com

MOSIS

Marina del Rey, CA

www.mosis.com Booth: 1509

From prototype to production, MOSIS is a design engineer's single source for a wide variety of semiconductor processes offered by major foundries (e.g. GF, IBM, TSMC).

Costs are kept low by combining designs from many customers into multi-project wafer (MPW) runs. With prototype costs reduced, engineers can submit several variations of the same design to the same run, thus shortening time-to-market.

Final designs can then be submitted to MOSIS for low- medium volume production or dedicated Engineering wafer runs (COT).

Along with wafers and die, MOSIS provides a full range of packaging and bonding options for designs fabricated through our service.

MunEDA GmbH

Munich, Germany

www.muneda.com Booth: 1725

MunEDA develops and licenses EDA tools and solutions that analyze, model, optimize and verify the performance, robustness and yield of analog, mixed-signal and digital circuits. Leading semiconductor companies rely on MunEDA's comprehensive WiCkeD™ tool suite – the industry's broadest family of advanced circuit analysis solutions – to reduce circuit design time and achieve maximum yield in their communications, computer, memory, automotive and consumer electronics designs. Founded in 2001, MunEDA is headquartered in Munich, Germany, with offices in Sunnyvale, California, USA (MunEDA Inc.), and leading EDA distributors in the U.S., Japan, Korea, Taiwan, Singapore, Malaysia, Scandinavia, and other countries worldwide. For more information, please visit MunEDA at www.muneda.com.

Nangate

Sunnyvale, CA

www.nangate.com

Nangate is an innovative developer of Electronic Design Automation (EDA) software and physical silicon intellectual property (IP) for Integrated Circuit design. Nangate offers software, IP and services for physical library IP creation, characterization, optimization and validation.

Booth: 1317

Nangate provides a unique alternative to one-size-fits-all standard cell libraries and a low-risk alternative to custom library development or full-custom chip design to improve performance, power and area.

Nangate's solution platform and IP integrates seamlessly with SoC design flows from the major EDA vendors.

National Instruments Corp.

Austin, TX

www.ni.com Booth: 1923

Engineers and scientists use National Instruments graphical system design tools to solve new and advanced control and automated test challenges. By using NI LabVIEW software to program embedded processors, field-programmable gate arrays (FPGAs), and I/O within NI hardware, design teams can abstract the complexity of their design without giving up flexibility and performance. By using off-the-shelf hardware instead of building a custom solution, engineers can prototype and deploy embedded monitoring and control solutions faster.

For more information, visit ni.com/embedded.

NEC Corp.

Kawasaki, Kanagawa, Japan

www.necst.co.jp/product/cwb/english/ Booth: 1223

CyberWorkBench, Behavioral C-Based synthesis and verification platform, enables not only a revolutionary reduction in ASIC/SoC/FPGA development time and costs; it improves the reliability and quality of the final product. The range of commercial products taped out during the last 20 years goes from network interface circuits, high-speed audio/visual signal processors for high-definition TVs and mobile phones, to cryptographic processors. CyberWorkBench has become an important key to a successful high-tech consumer electronics business that requires a short time-to-market.

NextOp Software, Inc.

Santa Clara, CA

www.nextopsoftware.com Booth: 3131

NextOp Software is focused on delivering assertion-based verification solutions that allow design and verification teams to uncover bugs, expose functional coverage holes, and increase verification observability.

NextOp's BugScope assertion synthesis is the first product to automatically generate functional assertions and coverage properties in SVA, PSL and Verilog formats. BugScope properties fit in existing simulation, formal, emulation and acceleration flows. BugScope can also be used to drive an effective functional review process.



Please Come Join Us!

TUESDAY, June 7, 12:00 pm - 2:00 pm | 25AB

IEEE CEDA: The Truths and Myths of Embedded Computing

Organizer: Dwight Hill, *Synopsys* **Speaker:** Shekhar Borkar, *Intel*

Computers have become ubiquitous, from powerful data centers housing supercomputing clusters to tiny microcontrollers in your toothbrush. However, the embedded-computing discipline does not get its fair share of attention. This talk will define the scope of embedded computing, compare it to general-purpose computing with appropriate metrics, challenge the myths that are floating around, and uncover the truths.

We will also discuss challenges in architecture, design, and test of future embedded computers, which will become even more ubiquitous as they become part of general-purpose computers.

WEDNESDAY, June 8, 5:00 pm - 5:45 pm | DAC Pavilion

Pistilli's Perspective: EDA Future – Feast or Famine?

Organizer: Shishpal Rawat, *IEEE CEDA*Chair: Thomas Pennino, *TP Technologies*Panelist: Pasquale (Pat) Pistilli, *MP Associates*

For almost 50 years, the EDA industry has bridged the productivity gap with every new process node adoption. Join Thomas Pennino, formerly of Bell Labs and DAC General Chair, for a discussion with Pat Pistilli, 2010 winner of the Phil Kaufman Award, on invention and reinvention of the EDA industry to meet the design challenges of the next half-century.

Booth: 2031

Booth: 2531

Oasys Design Systems, Inc.

Santa Clara, CA

www.oasys-ds.com

The leader in Chip Synthesis has the only product that can take full-chip RTL for today's largest chips and produce placed gates meeting tough design constraints. Oasys can handle 100 million gate chips in one pass and produces better results in a fraction of the time needed for traditional synthesis. RealTime Designer is tape-out proven and in production at leading-edge semiconductor companies. Visit the Oasys booth, 2031, to see why the top 10 semiconductor companies are moving to RealTime Designer.

OpenText

Richmond Hill, ON, Canada

connectivity.opentext.com Booth: 1205

The OpenText Connectivity Solutions Group, formerly Hummingbird, offers solutions that allow engineers to maximize the experience of their EDA environment: high-performance remote access to their EDA tools over LAN and WAN, complex 3D application display, team collaboration and productivity features. Every day, thousands of engineers depend on Exceed technologies to increase productivity, work with virtual teams around the world and shorten time to market. Come and visit us on Booth 1205 to discover how we can make your EDA experience phenomenally better.

Website: connectivity.opentext.com

OptEM Engineering Inc.

Calgary, AB, Canada

www.optem.com

OptEM Engineering's software and services focus on interconnect design, extraction, modeling and analysis for high-speed analog, digital, and mixed-signal ICs and cable/connector systems. For deep-submicron ICs, the OptEM Inspector software provides layout-to-circuit device extraction, and 2D/3D substrate and interconnect RC extraction for detailed analysis of crosstalk and delay effects at the cell level. For cable/connector systems, the OptEM Cable Designer software models high-performance multi-conductor flex, twisted-pair, and specialty cables in telecommunication and data transmission applications.

Orora Design Technologies, Inc.

Redmond, WA

www.orora.com Booth: 3214

Why search for FastSPICE with 10x speed up, while you can cut your mixed-signal simulation time by 100x to 1000x using the same simulator on the same test benches? Check out Orora's Arana, the industry-unique tool that automatically generates behavioral models from a netlist. For a complete solution of automating analog design and verification, stop by to see Orora's Arche Custom-IC Verification and Characterization Platform and Arsyn Automated Circuit Design and Reuse Platform.

Oski Technology, Inc.

Mountain View, CA

www.oskitech.com

Oski Technology is the world's only IC verification services company fully focused on formal verification. With 20 years of experience, Oski has pioneered and perfected a proprietary methodology to deliver complete verification solutions that transform the approach to RTL verification, properly integrating formal into traditional simulation-based and coverage-driven flows, and creating significant reductions in schedule and increased coverage, often finding corner-case bugs almost impossible to detect in a simulation environment. Oski's customers include Cisco, Cypress, NVIDIA, Rambus, Xilinx.

Booth: 1216

Booth: 2617

Booth: 1233

Physware, Inc.

Bellevue, WA

www.physware.com

Physware is a leading provider of high-speed and high-capacity 3D electromagnetic signal integrity, power integrity and EMI analysis field solutions for the microelectronics industry. The company's patented technology leverages the trend towards pervasive parallel Cloud Computing. Physware enables efficient and robust chip-package-system co-design while significantly reducing time-to-market. Physware's accelerated technology delivers unprecedented capacity handling, significantly faster speed than current methodologies, and the ability to span the entire design cycle in 3DIC, package and system simulations, while maintaining uncompromising Maxwell accuracy.

Polar Instruments Inc.

Beaverton, OR

www.polarinstruments.com Booth: 2021

Polar Instruments provides innovative, easy to use software tools for design and manufacture of PCBs. Polar's intuitive graphic interface and preconfigured structures allow quick and accurate board design cycles with complete documentation. Impedance control and signal integrity is our specialty. From lossy transmission line modeling, stackup design for rigid-flex boards to coupon generation. Detailed sensitivity analysis, extraction of RLGC matrices, s-parameters, graphing and more. Stop by our booth for a one month license and opportunity to win a monitor.

POLYTEDA Software Corp.

Santa Clara, CA

www.polyteda.com

POLYTEDA is the provider of accurate physical verification solutions with fast and predictable runtimes that are independent of hierarchy. The DRC/LVS tools are based on POLYTEDA's innovative One-Shot™ DRC technique, and its Fine-Grain Physical Verification™ technology platform. One-Shot DRC is different from the flat or hierarchical DRC technologies. It is architected to best address the most advanced process nodes with unparalleled accuracy, fast and predictable runtime response that exhibits a linear relationship with the number of objects to be processed.



Wednesday Cocktail Reception

6:00 - 7:00pm

Sails Pavilion





EXHIBITION HIGHLIGHTS

The 48th DAC exhibition is located in Halls D and H of the San Diego Convention Center.

Visit the DAC exhibition for an in-depth view of new products and services from nearly 200 vendors spanning all aspects of the electronic design process, including EDA tools, IP cores, embedded system and system-level tools, as well as silicon foundry and design services.

DAC PAVILION Hall D Booth 3421

The DAC Pavilion will feature 18 presentations on business and technical issues.

Sponsored by:





EXHIBITOR FORUM

Hall G in Booth 1005

The Exhibitor Forum provides a theater on the exhibit floor where exhibitors present focused, practical technical content to attendees. The presentations are selected by an all-user Exhibitor Forum Committee chaired by Magdy Abadir of Freescale Semiconductor, Inc. Each session is devoted entirely to a specific domain (e.g., verification or system-level design) and consists of presentations from three companies.

Topics include: System-Level Design/Embedded Software, Physical Design and Sign-Off, Verification, Power Management/Signal Integrity, Analog/Mixed-Signal and RF, Design for Manufacturability, Intellectual Property Cores, Design for Test and Manufacturing Test, Package Design, and Silicon Validation and Debug.



ESS

Hall F of the Exhibit Floor

Visit the new Embedded Systems and Software (ESS) Zone in Hall F of the exhibit floor to see the latest embedded systems, IP and SoC products and services. The ESS Zone on the DAC exhibit floor offers attendees the combination of a focused area to find products and services for the design of embedded systems, as well as a theater featuring product teardowns and presentations by a host of ESS Zone embedded systems, IP and SoC exhibitors. Theater presentations are 30-minutes each and offer an in-depth look into systems used to power multicore designs, develop products on open source platforms such as Android, best practices for integrating IP into your SoC designs; plus product teardowns of today's most interesting electronics brought to you by iHS iSuppli. Stop by booth 1825 or visit the DAC website for the complete schedule of presentations.

ESS EXHIBITORS (AS OF 5/12/2011)

| ARM, Inc. | 1323 |
|-------------------------|------|
| Carbon Design Systems | 1914 |
| CoFluent Design | 1815 |
| Cortus S.A. | 1814 |
| IBM Corp. | 1818 |
| iHS iSuppli | 2319 |
| Laflin/Instigate | 1924 |
| Mentor Embedded: | |
| Freescale Semiconductor | 1821 |
| MIPS Technologies, Inc. | 1718 |
| NetLogic Microsystems | 1720 |
| Texas Instruments | 1819 |
| National Instruments | 1923 |
| Proximus DA | 1925 |
| STM Products/EDALabs | 1920 |
| Vayabya Labs | 2019 |
| | |

EXHIBIT-ONLY PASS

Register for an exhibit-only pass and receive admission to all days of the exhibition, all Keynotes, all DAC Pavilion, Exhibitor Forum sessions, Embedded Systems and Software sessions and the three evening receptions.

EXHIBITION HOURS

| Monday, June 6 | 9:00am - 6:00pm |
|-------------------|-----------------|
| Tuesday, June 7 | 9:00am - 6:00pm |
| Wednesday, June 8 | 9:00am - 6:00pm |



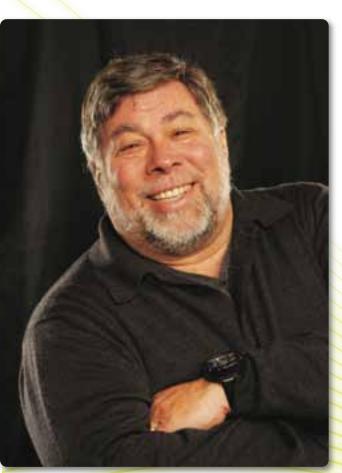
MONDAY KEYNOTE ADDRESS

Up Close and Personal with Steve Wozniak

Monday, June 6

2:00 - 3:00pm

Room: 20AB



Speaker: Steve Wozniak - Fusion-io, San Jose, CA

Steve Wozniak will be interviewed live on stage by San Jose Mercury News columnist Mike Cassidy on a wide range of topics, including the 'joy' of engineering and following your passion to convert innovative ideas into reality. Steve will provide a unique insight into the vision that started the largest and most successful technology company in the world.

Sponsored by:



Prolific, Inc.

Newark, CA

www.prolificinc.com Booth: 2331, 2424

Prolific's products automate creation of standard cells and optimization of physical designs. ProPower® and ProTiming™ run after place-and-route, reducing leakage by 25%-70% on previously optimized designs, and improving TNS and WNS by 10%. ProDFMOptimize™ improves manufacturability during thelibrary creation process. ProGenesis® automates standard cell creation at 28nm and above, while library designers currently use ProGenesis® Elite to create libraries for the 20nm node. Both reduce development time, allow architectural exploration, and automatically adapt to changes in design requirements or rules.

ProPlus Design Solutions, Inc.

San Jose, CA

www.proplussolution.com Booth: 2025

The Silicon Valley-based start-up develops cutting-edge technologies to enhance the linkage between design and manufacturing, and delivers innovative EDA solutions for DFY. It is based on the Device Modeling Platform that has been the choice for leading semiconductor companies since mid-90s, and the Circuit Design and Electrical Verification Platform targeted to meet the challenges of performance and yield trade-offs for advanced circuit designs.

ProPlus has R&D centers in both the US and China, branch offices in Tokyo, Hsinchu and Shanghai.

ProximusDA

Munich, Germany

www.proximusda.com Booth: 1925

ProximusDA delivers products for system level architects, verification engineers and embedded software developers facing the heterogeneous parallel computing challenge. ProximusDA solutions extend the hardware transaction level methodology to embrace the software side providing a unified transaction level abstraction of the HW/SW system. ProximusDA's fast lightweight distributed task scheduling technology is used in the products portfolio and as a software IP stack for the embedded market.

Pulsic Inc.

Santa Clara, CA

www.pulsic.com Booth: 2214, 2318

Pulsic is the premier provider of physical design tools for custom digital and AMS designs. Pulsic's UnityTM is a fully integrated production-proven solution for floorplanning, placement, and routing of extreme design challenges at advanced nodes. Unity delivers handcrafted quality, faster than manual design. Pulsic has delivered successful tapeouts at 40 nm and below for IDMs and fabless customers in memory, FPGA, custom digital, LCD, imaging, processor and AMS markets worldwide. For more information visit http://www.pulsic.com

Quest Product Development Corp.

Arvada, CO

www.quest-corp.com

Quest has designed, developed, & manufactured 300+ medical devices & scientific systems.

Booth: 2014

Booth: 1607

Booth: 1610

R3 Logic Inc.

Bedford, MA

www.r3logic.com

R3Logic has been a pioneer in EDA tools for 3D system and IC design. With our flagship product, R3Integrator, we offer a truly plug-and-play solution to allow you to maximize IP re-use in 3D Systems-in-Stack without changing your current design flow. OpenAccess-based R3Integrator features automated TSV assignment, initial floor-planning, multi-grid routing, package/chip/interposer co-design, and physical vs. logical verification. Let us show you how you can reap the power and performance benefits of 3D integration.

Rapid Bridge

San Diego, CA

www.rapidbridge.com

Rapid Bridge focuses on the application of its technology and services to solve the industry's dilemmas of cost, performance, power and time to market. The Technology Division focuses on the advancement and application of our patented technologies including LiquidIP™, LiquidASIC™, LiquidSoC™ and Core Power Reduction (CPR™) Technology. The Design Services Division delivers front-to-back digital design and chip design services for mixed-signal and SoC projects. Rapid Bridge's worldwide presence, exceptional combination of experience, expertise and technology access provides us with a unique ability to offer our clients a shorter time to market, unparalleled quality and overall value creation. Visit us at www.rapidbridge.com.

Real Intent, Inc.

Sunnyvale, CA

www.realintent.com Booth: 2131

Real Intent is the leading provider of software products that accelerate Advanced Sign-off Verification of electronic designs. The company provides comprehensive Clock Domain Crossing solutions for ensuring synchronization between on-chip IP cores, as well as advanced RTL and Constraint Analysis solutions for detecting and eliminating potential complex failure modes of today's highly integrated SoCs. Real Intent's products lead the market in high performance, capacity, report accuracy and comprehensiveness, enabling fast and complete sign-off. For more information, please visit www.realintent.com.



Visit the Food Court area in Hall G for a chance to



Booth: 2325

Booth: 1606

Booth: 2631

Reveal Design Automation

Ann Arbor, MI

www.reveal-da.com

Reveal Design Automation is revolutionizing the way formal verification is used for complex microprocessor and microcontroller designs. Reveal's patent-pending, massively scalable Architecture Validation solutions supplant current ad-hoc methods for establishing compliance of a microarchitectural implementation to its ISA specification. Orders of magnitude faster and more scalable than traditional formal approaches, Reveal's proprietary technology can quickly pinpoint discrepancies between different implementations of an ISA or establish their functional equivalence with minimal user intervention.

Rocketick

Ramat Gan. IL

Booth: 2914 www.rocketick.com

Functional verification is a severe bottleneck in chip design projects. Rocketick's flagship product, RocketSim, solves functional verification bottlenecks by complementing simulators with a GPUbased acceleration solution, offering over 10X faster simulations for highly complex designs and 5X server-memory savings. RocketSim offers outstanding coverage and capacity, allowing teams to tape-out more complex products, much earlier, and with much greater confidence.

RTC Group - EDA Tech Forum

San Clemente, CA

www.rtcgroup.com

RTC magazine spotlights trends and breakthroughs in the design, development and technology of embedded computers. The publication offers broad based technical, product and marketcoverage of the embedded computer arena to industry decision makers. With strong market analysis and technical content, RTC is the magazine engineers and managers rely on for timely coverage of this developing and expanding industry. We offer FREE subscriptions for qualified subscribers.

Runtime Design Automation

Santa Clara, CA

www.rtda.com

RTDA helps companies of all sizes meet schedules despite increased design complexities and larger workload. Our family of products enables you to do more with less. LicenseMonitor makes your expensive tool license usage visible. LM also does your next year forecast/budget according to your projects roadmap. NetworkComputer, the fastest job scheduler removes bottlenecks in execution. FlowTracer maximizes design productivity & licenses by deploying fully automated standardized repeatable parallel flows. WorkloadAnalyzer simulates your what-ifs: should I buy more small machines or less tool licenses?

S2C Inc.

San Jose, CA

www.s2cinc.com

S2C is demonstrating its rapid FPGA-based prototyping system that accelerates SoC/ASIC prototype development. This system is based on S2C's TAI LogicModules (Altera and Xiliinx), S2C's prototyping design automation software, and S2C's family of Prototype Ready™ IP, Accessories, and Platforms.

Booth: 3124

Booth: 1432

Booth: 3317

Booth: 1404

S2C's 4th generation technology features larger capacity, highperformance, debugging designs in multiple FPGA concurrently and C-APllink with high-level tests in PC. These new features enable designers to quickly assemble SoC prototypes, enabling anearly start on software development.

Sagantec

Santa Clara, CA

www.sagantec.com

Solutions for custom IP design, proven to cut layout time and effort by factors of 3x to 20x.

Migration of analog, mixed-signal and memory IP to the next process technology, or between foundries. Covering all advanced processes nodes of 40nm, 32nm and including the migrationchallenging 28nm technology.

Automatic DRC correction and guick layout update following change of foundry design rules, PDKs, and automatic implementation of recommended DFM rules.

SAME

Sophia Antipolis, France

www.same-conference.org

SAME: Sophia Antipolis MicroElectronics

SAME's Mission:

Valorize, promote and develop excellence in the microelectronics sector covering the design technology for advanced electronic circuits in the Alpes-Maritimes (French Riviera), South of France.

SAME organizes one of the major European microelectronics events: the SAME Forum, with the support of all major EDA and semiconductor companies.

SAME 2011 Forum

Main Topic: Digital Mobility, Any Time, Any Where, Any Content,

Any Device

October 12 & 13, 2011 at Sophia Antipolis, France.

Information on www.same-conference.org

Samsung Electronics

San Jose, CA

www.samsung.com

Samsung's foundry business supports fabless and IDM semiconductor companies with advanced IC design requirements through foundry, ASIC or COT engagements by offering full service solutions encompassing design kits and proven IP to full turnkey manufacturing. Currently in mass production at 45nm, Samsung Foundry is also ready for next generation designs at 32/28nm and beyond by leveraging deep expertise in advanced process technologies, design technologies, as well as a long, proven track record in high-volume manufacturing. For more information, visit www.samsung.com/Foundry.

The ever popular EDA Tech Forum is now TECH DESIGN EDA Tech Forum is now TECH DESIGN EDA Tech Forum is now TECH DESIGN EDA Tech Forum is now Tech Forum is now Tech DESIGN EDA Tech Forum is now Tech Forum is now Tech DESIGN EDA Tech Forum is now Tech Forum is now Tech DESIGN EDA Tech Forum is now Tech Forum is now Tech Period (Fig. 1988).

NEW 2011 JOURNAL

Tech Design Forum is on the Front Line Delivering Tools, Techniques and Information Giving Our Readers the Necessary Abilities to Streamline Processes and Succeed in Today's Market.

The magazines will continue to cover the entire design flow – but each edition will provide extra coverage in specific focus areas such as functional verification, embedded software, physical IC design, design for manufacturing and printed circuit boards.

The TECH DESIGN
FORUM offers technical information in an efficient, compact and focused format.

SUBSCRIBE TODAY:

WWW.EDATECHFORUM.COM

Booth: 3125, 3224

Satin Technologies

Montpellier Cedex 2, France

www.satin-tech.com

Satin Technologies delivers software solutions for fact-based design quality monitoring and closure. Working within customers' design flows, the company's VIP Lane® turns customers' design practices (for IP blocks, SoCs, embedded systems) into a robust and reliable set of quality criteria and metrics. These customer-based parameters are used to create automated, sharable dashboards and quality compliance reports. Providing an alternative to manually filled, time-consuming checklists and documents, VIP Lane® shortens time-to market by delivering effective flow integration and on-the-fly quality monitoring at zero overhead to design teams.

Seloco, Inc.

Songpa-dong, Songpa-gu, Seoul, South Korea

www.seloco.com Booth: 2727

Since 1990, MyCAD offers a Windows-based EDA toolset installed in thousands of copies around the world – America, Europe, Asia recently including China and India. The main product for industrial application is MyChip Station, a set of IC layout editing and verification tools. MyCAD tools' economical, handy and practical features have encouraged small to medium size designs of ICs, LEDs, Opto-devices, MEMs, and LCDs recently. MyChip Station is also used to convert AutoCAD data to photolithographic mask data generation. A new feature is its added cross section view capability for an IC/device layout. MyCAD's educational tool set includes VHDL simulator/synthesizer, schematic capture/logic simulator, SPICE simulator and an FPGA experimental kit. Try free at www. mycad.com

Semifore, Inc.

Mountain View. CA

www.semifore.com Booth: 3239

Semifore Inc., "The Addressmap Experts," provides the CSRSpec language and the CSRCompiler, a complete register design solution for hardware, software, verification, and documentation. Collaboratively manage your design from a single source specification. CSRSpec, SystemRDL, IP-XACT, or Spreadsheet inputs generate: Verilog and VHDL RTL; Verilog, or C headers; Perl, IEEE IP-XACT; System Verilog for UVM, VMM and OVM; HTML web pages; and Word or Framemaker documentation. Only Semifore gives your entire team a complete, correct, up-to-date addressmap verification ecosystem.

Si₂

Austin, TX

www.si2.org Booth: 1631

Si2 is the largest organization of industry-leading semiconductor, systems, EDA and manufacturing companies focused on the development and adoption of standards to improve the way integrated circuits are designed and manufactured, in order to speed time-to market, reduce costs, and meet the challenges of sub-micron design. In our booth this year, member companies will be demonstrating products which implement the standards which Si2 Coalitions have developed.

Sigrity, Inc.

Campbell, CA

www.sigrity.com

Sigrity provides advanced software analysis solutions to ensure power integrity and signal integrity in chips, packages and printed circuit boards; and physical design tools for single die and SiP implementations. Over 250 companies utilize Sigrity products as part of industry standard design flows. Sigrity solutions help companies overcome design challenges and get to market faster while avoiding costly respins and field failures. Sigrity products have won technology innovation awards and the company receives high marks for customer support.

Booth: 2525

Booth: 3017

Booth: 3025

Silicon Frontline Technology

Campbell, CA

www.siliconfrontline.com

At DAC, Silicon Frontline will demonstrate its newest Guaranteed Accurate post-layout verification solutions that reduce post-layout verification time and reduce time to quality silicon.

- H3D, the industry's first hierarchical extractor with field solver accuracy and unmatched performance and capacity
- R3D, the leading power device analysis solution, with capabilities that deliver a more efficient design
- F3D with its fast XL option for Guaranteed Accurate AMS design

www.siliconfrontline.com

SKILLCAD Inc.

San Jose, CA

www.skillcad.com

SKILLCAD is dedicated to custom routing and productivity enhancement tools for IC layout design.

SKILLCAD Layout Automation Kit delivers advanced modules for bus/path routing (stepRouter), auto via dropping, pin/label placement, net tracing, guardring, shielding, metal slotting and dummy pattern fill etc. The newly released V-Editor integrates separate layout editing steps of shape selecting, pushing and design rule enforcing into one step, minimizes mouse clicks in polygon pushing and bus/net editing. Our customers get 30+times speed gain with SKILLCAD Custom Layout Kit. SKILLCAD Custom Layout Kit is seamlessly integrated into Cadence Virtuoso Platform, supporting both IC5 and IC6.

SKILLCAD Flat Panel Layout Editor introduces the first full solution for TFT LCD layout design into Cadence Virtuoso platform. rRouter handles hundreds of connections simultaneously and automatically adjusts routing width and wiggle patterns to meet constrains of resistances (equal or distributed). rChecker accurately measures resistance of path/polygon connections and provides utilities/interface to analyze the resistance deviation. Our customers get better routing result (less resistance deviation) with rRouter and rChecker than the result from other company's tools. There are many other tailor-made utilities in the SKILLCAD Flat Panel Layout Editor.

Booth: 2018

Booth: 3138

Booth: 2826

Booth: Lobby

SmartPlay Inc.

San Jose, CA

www.smartplavin.com

SmartPlay provides design services in IC Design

(verification, physical design, analog design), and Embedded Software services. We are staffed with over 450 engineers worldwide spanning US and India. We offer DV, PD, and Analog Turnkey and on-site design services. We have 130 Design Verification and 100 Physical Design engineers available to support your requirements. Languages supported include SystemVerilog, C/C++ and Verilog with OVM, RVM and VMM methodology experience. SOC and IP verification experience including PCI-E, USB, DDR, HDMI, SERDES and ARM / MIPS / ARC verification. Support for Cadence, Synopsys, Magma, Mentor and Atoptech flows.

Solido Design Automation Inc.

San Jose, CA

www.solidodesign.com

Solido provides variation-aware custom IC design software. Solido Variation Designer is used by leading semiconductor companies to reduce design and manufacturing costs by improving parametric yield and designer productivity while enhancing design performance.

Variation Designer analyzes and debugs variation caused by process and environmental (PVT) corners, global and local random variation, and layout-dependent effects. It is used by analog/ mixed-signal/RF, I/O, memory and standard cell digital designers. Variation Designer is qualified by TSMC and STARC, and is integrated with leading custom design tools.

Sonnet Software, Inc.

N. Syracuse, NY

www.sonnetsoftware.com

Sonnet Software provides high frequency electromagnetic (EM) software for 3D planar circuit and component model extraction. The Sonnet Suites are aimed at today's demanding design challenges involving predominantly planar circuits and antennas (including microstrip, stripline, coplanar waveguide, PCB (single and multiple layers) and RF packages incorporating any number of layers of metal traces embedded in stratified dielectric material. Sonnet integrates with most major EDA design flows. Visit Booth 2826 for information on Sonnet's latest software Release 13.

Springer

New York, NY

www.springer.com

Get hands-on experience with Springer's multi-format publishing model: print - eBook - MyCopy (printed eBooks for \$24.95).

Stop by our booth and browse our books in your preferred format.

With more than 4500 books currently available in the Engineering eBook Collection, our mission is to support your research. Ensure optimized print and electronic dissemination of your work, too!

Get Read, Publish With Springer,

SpringSoft, Inc.

San Jose, CA

www.springsoft.com

SpringSoft provides automation technologies that accelerate engineers during the design, verification and debug of complex digital, analog and mixed-signal designs. Our award-winning products provide engineers with the power to achieve functional closure for verification and maximize performance and innovation for custom IC design. Solutions include the Verdi™ Automated Debug System, the Certitude™ Functional Qualification System, and Laker™ Custom IC Design products. Our latest solution, the ProtoLink™ Probe Visualizer gives engineers the visibility required to significantly cut their prototype debug time.

Silver Exhibitor

Booth: 2043

Booth: 2926

Booth: 1920

Booth: 2425

StarNet Communications

Sunnyvale, CA

www.starnet.com

StarNet will demonstrate how its line of X Server clients for Windows, Mac, Linux and iPad systems is faster, more affordable and more secure than solutions like VNC and Exceed on Demand.

Using the LIVE Connections, EDA users can connect to their tools from a Windows PC and reconnect from a Mac or even iPad with LAN-like performance.

STM-Products/EDALab

Verona, IT

www.stm-products.com

Two innovative embedded systems verification frameworks are presented at this DAC edition: radCHECK and HIFSuite.

radCHECK allows any embedded software designer to use property-based verification.

A guided property editor and an automatic test cases generator have been integrated in a single tool for effective, but very simple, dynamic verification.

HIFSuite allows to escape from the HDL babel by automatically translating heterogeneous models (VHDL, verilog, SystemC, StateFlow, C/C++) into a homogeneous SystemC representation, automatically abstracted into TLM and C++ for dynamic verification.

Synapse Design

San Jose, CA

www.synapse-da.com

Synapse Design is the preferred design partner of many Fortune 500 System & Semiconductor companies around the world.

Founded in 2003, headquartered in San Jose with operations in Irvine, Boston, San Diego, Colorado, China, India and Europe. Synapse offers full turnkey solutions or deployment of large teams world-wide. We support our clients from architecture to GDS including analog IP and embedded software development.

We specialize in assisting our clients in developing their next generation ICs, across many product domains.

Synchronicity see Dassault Systèmes

Lowell, MA

www.3ds.com Booth: 1625

See Dassault Systemes at Booth #1625

Synopsys, Inc. - Corporate

Mountain View, CA

Platinum Exhibitor 3
Booth: 3433, 3445

Booth: 3328

www.synopsys.com

Fast Forward to Predictable Success with the EDA software, intellectual property (IP) and services needed to meet today's ever increasing time-to-market semiconductor design and manufacturing demands. With the explosion of "smart" consumer devices driving design needs, Synopsys' comprehensive portfolio of integrated system-level, implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions can help designers address their key design and manufacturing challenges. Visit Synopsys at DAC or www.synopsys.com to put your next design on fast forward to predictable success.

Synopsys, Inc. -The Standards Booth

Mountain View, CA

www.synopsys.com

Synopsys, Inc. - The Standards Booth

www.accellera.org, www.ieee.org, www.ieee-isto.org, www.iplnow.com, www.mipi.org, www.systemc.org

Interoperability based on open standards and teamwork leads to greater productivity for successful design projects. Synopsys sponsors this booth to promote industry standards that provide increased productivity, reduced cost and improved EDA interoperability. See the latest advancements in the industry for system, open verification, and interoperable PDK standards and ecosystems. Also, visit with IEEE-ISTO to learn about advancing technology standards with MIPI Alliance, LTAB, and IMTAB.

Synopsys, Inc. - Partner Booth

Mountain View, CA

www.synopsys.com Booth: 3334

32nm and 28nm Ready, from Concept to Proven Silicon

Proven design, IP and manufacturing solutions for 32nm and 28nm ARM-Powered® smart consumer devices are available today through a unique design engagement between ARM, GLOBALFOUNDRIES, IBM, Samsung Electronics and Synopsys.

Combining industry leadership in fast models, virtual prototyping, interface, physical and processor IP, and design tool/flow solutions for the Common Platform Technology Alliance 32nm and 28nm high-k metal-gate (HKMG) process technologies, results in early software development and a silicon proven path to reduce time to market, lower system cost and design risk.

SynTest Technologies, Inc.

Sunnyvale, CA

www.syntest.com

Since 1990, SynTest has developed and commercialized many market-leading design-for-test (DFT) products, including Logic/Memory BIST (TurboBIST), Scan/ATPG (TurboScan), test compression (VirtualScan), and fault simulation (TurboFault). SynTest's DFT IP, e.g., at-speed scan/BIST, are silicon-proven and protected by a rich portfolio of 38+ patents. The TurboBIST-Logic product is used today by leading companies to reduce test-cost and improve quality. The newly released RobustScan product provides Framework for Logic and Memory Soft-Error Protection. SynTest tools are backed by the most dedicated support team.

Booth: 2625

Booth: 2231

Booth: 2227

Booth: 1305

Tanner EDA

Monrovia, CA

www.tannereda.com

Tanner EDA provides Windows and Linux based EDA software solutions that drive innovation for the design, layout and verification of analog and mixed-signal ICs and MEMs. Tanner EDA's HiPer Silicon is a complete IC design suite that encompasses schematic capture, circuit simulation, waveform probing, physical layout, foundry-compatible DRC, extraction, and verification. Tanner EDA products enable faster time to market, lower costs, and shorter design cycles and are used to develop devices in the biomedical, consumer electronics, next-generation wireless, imaging, power management and RF markets.

Target Compiler Technologies NV

Leuven, Belgium

www.retarget.com

Target is the leading provider of tools for the design, programming and verification of application-specific processors (ASIPs) in (multicore) systems-on-chip. Target's tools enable the design of ASIPs with performance and energy characteristics close to hardwired datapaths. Yet these ASIPs provide software programmability, thus permitting changes in specifications and extending the revenue lifetime of SoCs. IP Designer supports ASIP architectural exploration, and generates a complete C compiler based software development kit as well as a low-power hardware implementation for each ASIP.

Teklatech

Copenhagen, Denmark

www.teklatech.com

Teklatech drives innovation in Power Integrity and Power Noise optimization to reduce IR-Drop, noise and EMI early in the backend flow.

FloorDirector allows designers to improve Power Integrity significantly by reducing dynamic current peaks and shaping the slope. FloorDirector can reduce Power Noise in custom frequency bands, thereby improving performance and robustness of RF, mixed-signal and EMI-challenging designs. FloorDirector is highly automated, non-intrusive to the existing flow and integrates seamlessly into all major ASIC backend flows.



User Track

FOR EDA USERS, BY EDA USERS

The DAC User Track brings together IC designers from across the globe. The technical program offers a unique opportunity to pick up the latest tips and tricks from the industry expert IC designers. UT features over 110 presentations on a wide variety of EDA topics. There is no other way to improve your 'design IQ' in just a short amount of time.



Tiempo

Montbonnot St Martin, France

Booth: 3039, 3041 www.tiempo-ic.com

In the Tiempo booth, the company will be presenting demonstrations of its ACC (Asynchronous Circuit Compiler) tool and timing-driven place-and-route flow with Synopsys PrimeTime and ICC. Tiempo will also demonstrate the operation of actual chips developed using Tiempo technology.

In the Tiempo suite, application engineers will be presenting overviews of Tiempo technology, as well as conducting in-depth tutorial workshops on their usage.

Please visit the Tiempo booth, or www.tiempo-ic.com to reserve a place in any of these educational sessions. Space is limited.

TinnoTek Inc.

Hsinchu City, Taiwan

www.tinnotek.com.tw Booth: 3021

Taiwan-based TinnoTek Inc. specializes in EDA tools for SoC designs, including (1) SoC Power Estimation Tools (100X faster than gate-level power simulation with sing-off accuracy), and (2) World's first All-Digital Cell-Based PLL Compiler, namely eClock.

TOOL Corp.

Tokyo, Japan

www.tool-corp.com Booth: 2126, 2226

TOOL Corp. provides innovative EDA solutions to meet your IC backend design needs. Showcased is LAVIS, provides rich functionality including fast power-line resistance calculation, timing closure analysis, layout verification and failure analysis built on high-performance data handling & visualization engine. In addition, OASIS-Utility, a unique set of tools including a fast hierarchical data checker against rigorous custom sign-off regulations is exhibited. Using LAVIS and OASIS-Utility can minimize risks in data logistics situations through quick verification of illegal data.

Tower Jazz

Newport Beach, CA

www.towerjazz.com **Booth: 2024**

TowerJazz provides design kits, IPs and dedicated design services for its process technologies for first-time working silicon and fast time-to-market. TowerJazz belongs to the IPL Alliance to deliver interoperability of process design kits (iPDKs) for its customers' analog/mixed-signal designs. TowerJazz has partnerships with every major EDA vendor and with IP providers to supply its customers with the most comprehensive and up-todate design solutions and it has qualified reference flows for its 180nm power management process with several EDA vendors. www.towerjazz.com

True Circuits, Inc.

Los Altos. CA

www.truecircuits.com

True Circuits, Inc. (TCI) is the leading provider of timing IP for the semiconductor, systems and electronics industries. TCI develops robust state-of-the-art circuits using a methodical and proven design strategy and in close association with the world's leading fabs, IDMs and design service providers. TCI offers a complete family of high quality, low-jitter and standardized PLLs and DLLs in a range of frequencies, multiplication factors, sizes and functions in TSMC, GlobalFoundries, UMC and Common Platform processes from 180nm to 28nm.

TSMC

San Jose, CA

Booth: 2535, 2648

Gold Exhibitor

Booth: 3349

Booth: 2849

www.tsmc.com

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Aachen, Germany

www.umic.rwth-aachen.de Booth: 3321

UMIC is a research cluster focusing on the demands of future mobile applications and systems. Activities cover research on basics concepts and new paradigms, the development of tools, prototypes and demonstrators, and the technology transfer to industry.

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EnSilica - IP SoC Village

Wokingham, United Kingdom

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iHS iSuppli

El Segundo, CA

www.isuppli.com Booth: 2319

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Lewisville, TX

www.texEDAdesign.com Booth: 3119

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