DESIGN AUTOMATION CONFERENCE

June 13-18, 2010
Anaheim Convention Center

ANAHEIM

Sponsored by:

SIGDA special interest group of ACM design automation

CEDA IEEE Council on Electronic Design Automation

EDA CONSORTIUM

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GENERAL CHAIR'S WELCOME

Dear Colleague:

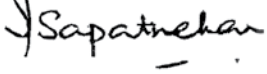
It is a great pleasure to welcome you to the 47th edition of the Design Automation Conference in Anaheim. As the central "meeting place" for electronic design and design automation where the industry puts on its grand annual show, there are many facets to DAC. It's the place where new contacts are made, where deals are sealed, where theory meets practice, where colleagues across the industry network, where the seeds of great new ideas are sown – and much more. DAC is our annual signpost that points the way to the future.

As organizers of the event, we work with DAC's sponsors and hundreds of volunteers to make it worth your time to attend. This year, in addition to reinforcing traditional strengths, we have added a number of exciting new elements. Here's a sample of what the 47th DAC brings to you:

- The keynote lineup features three distinguished and accomplished industry luminaries: Doug Grose, CEO of GLOBALFOUNDRIES will address the central role of the foundry in electronic design on Tuesday. Bernie Meyerson, Vice President for Innovation at IBM Corporation, will discuss his vision for next-generation IT infrastructure for EDA and the move towards cloud computing. Finally, Iqbal Arshad, Corporate Vice President of Innovation Products at Motorola, will overview his experiences in driving the Motorola Droid from concept to product.
- A vibrant exhibition showcases nearly 200 companies, including all of the largest EDA vendors and a significant foundry presence. The Exhibitor Forum theater features focused technical presentations from exhibitors, while IC Design Central's exhibit area and a presentation stage bring together the entire ecosystem for SOC enablement, including IP providers, design services providers, and foundries.
- DAC hosts a special Embedded/SOC Enablement day on Thursday to further advance the partner eco-system. It attracts a mix of chip creators, ecosystem suppliers, and research-focused participants.
- A robust and exciting technical program includes an exciting array of panels and special sessions that complement a carefully selected subset of the contributed research papers.
- The User Track program, specifically designed for EDA tool users, features presentations and poster sessions that highlight outstanding solutions to critical design and methodology challenges, and case studies of innovative tool use. In its second year, it is 50% larger than last year's acclaimed program.
- An excellent slate of tutorials covers topics such as low-power design, ESL, and software development for the EDA professional.
- Management Day includes invited presentations and networking opportunities for decision-makers in the industry, and highlights issues at the intersection of business and technology.
- An impressive constellation of fourteen colocated events and six DAC workshops complements the DAC program: this includes established conferences and symposia such as AHS, DFM&Y, DSNOC, HOST, HLDVT, NANOARCH, SASP, and SLIP, as well as meetings on emerging topics such as bio-design automation, mobile/cloud computing, and smart grids.

As you can see, there's tons of good stuff in here – I am sure you will have a fruitful time in Anaheim!

Sachin S. Sapatnekar
General Chair, 47th DAC



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ACM is an educational and scientific society uniting the world's computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. For more information, please visit http://www.acm.org.

The ACM Digital Library is the definitive online resource for computing professionals. Fully integrating the ACM Guide to Computing Literature, it provides access to ACM's complete collection of publications and bibliographic citations from the universe of published computing literature. http://www.acm.org/dl.

Additionally, ACM has 34 Special Interest Groups (SIGs) that focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as DAC, SIGGRAPH, OOPSLA, SC and CHI, providing attendees the opportunity to meet experts in their fields of interest and network with other knowledgeable members. http://www.acm.org/sigs.

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ACM/SIGDA

ACM/SIGDA (Special Interest Group on Design Automation) has a tradition of over forty years of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASPDAC, plus approximately 15 smaller symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the Univ. Booth and Ph.D. Forum at DAC and the CADathlon at ICCAD, and funds various scholarships and awards. SIGDA provides its members with full access to SIGDA-sponsored conference proceedings in the ACM Digital Library and the SIGDA E-Newsletter containing information on upcoming conferences and funding opportunities, emailed to SIGDA members regularly. The SIGDA E-Newsletter also includes SIGDA News which highlights the most relevant events in the EDA and semiconductor industry, and the "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation. SIGDA has recently initiated the creation of Technical Committees in various areas of EDA, ranging from Physical Design and Logic Synthesis, to System-Level Design, Low-Power Design, Reconfigurable Computing, Testing, Verification, and Emerging Technologies. 13th Ph.D. Forum Member Meeting on Tuesday evening to find out how the Technical Committees provide a link between Wednesday evening SIGDA activities and various technical areas in EDA. SIGDA also provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems). For further information on SIGDA's programs and resources, see http://www.sigda.org. In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org.

As an EDA professional, isn't it time YOU joined SIGDA?

IEEE/COUNCIL ON ELECTRONIC DESIGN AUTOMATION

The IEEE Council on Electronic Design Automation (CEDA) provides a focal point for EDA activities spread across six IEEE societies (Antennas and Propagation, Circuits and Systems, Computer, Electron Devices, Microwave Theory and Techniques, and Solid State Circuits). The Council sponsors or co-sponsors over a dozen key EDA conferences, including the Design Automation Conference (DAC) and the International Conference on Computer Aided Design (ICCAD), Design Automation and Test in Europe (DATE) and events at Embedded Systems Week (ESWeek). The Council also publishes IEEE Transactions on CAD, as well as the IEEE Embedded Systems Letters. Since its founding, the Council has expanded its support of emerging areas within EDA such as smart power grid, sponsored new initiatives including the Distinguished Speaker Series and is increasing recognition to members of the EDA profession via awards such as the A. Richard Newton and Phil Kaufmann Awards. The Council welcomes new volunteers and local chapters. For more information on CEDA, visit: www.c-eda.org.

EDA CONSORTIUM

The EDA Consortium (EDAC) is the international industry association for the providers of tools, IP, and services that enable engineers to create the world's electronics products. Its mission is to promote the health of the EDA industry by addressing common industry needs and providing valued services. By publishing the Market Statistics Service (MSS) EDAC enables worldwide tracking of EDA, Semiconductor IP and services revenue. By co-sponsoring the prestigious annual Phil Kaufman Award, the EDA Consortium and the IEEE Council on EDA bring industry-wide recognition to distinguished contributions to EDA. As a co-sponsor of DAC and DATE, the EDA Consortium represents the interests of exhibiting companies. EDAC members influence industry initiatives by participating on committees to address common needs as well as play a positive role in reducing costs for the industry and its customers.

Examples of committee accomplishments include an EDA operating systems roadmap, anti-piracyeducation, licensing guidelines, and the reduction of governmental export controls. EDAC offers international forums and symposiums which are well attended by industry CEOs, executives, press, and analysts. These events cover topics of interest to emerging and large EDA companies alike. EDA Consortium members receive a 10% discount on DAC booth/suite space. For more information call 408-287-3322 or visit www.edac.org. EDAC is located in San Jose, CA, USA.

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IMPORTANT INFORMATION AT-A-GLANCE

EXHIBIT HOURS

Monday, June 14	9:00am - 6:00pm
Tuesday, June 15	9:00am - 6:00pm
Wednesday, June 16	9:00am - 6:00pm

CONFERENCE REGISTRATION HOURS

Sunday, June 13	7:30am - 6:00pm
Monday, June 14	7:00am - 6:00pm
Tuesday, June 15	7:00am - 6:00pm
Wednesday, June 16	7:00am - 6:00pm
Thursday, June 17	7:00am - 6:00pm
Friday, June 18	7:00am - 4:00pm

TUTORIAL REGISTRATION

Monday Tutorial Registration

Monday, June 14, 7:00am - 6:00pm

You may register for tutorials at Conference Registration located in the Main Lobby.

Friday Tutorial Registration

Friday, June 18, 7:00am - 4:00pm

Sunday through Thursday, you may add a Friday tutorial at Conference Registration located in the Main Lobby. Beginning Friday morning, at 7:00am, Tutorial Registration will be located adjacent to room 208AB on the 2nd floor.

47TH DAC PROCEEDINGS DVD

Additional copies of the 47th DAC Proceedings DVD may be ordered prepaid from:
ACM Order Department
P.O. Box 11414, New York, NY, 10286-1414
Phone: +1-800-342-6626 (US and Canada)
Phone: +1-212-626-0500 (Global)
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STAY CONNECTED AT DAC

Wireless Internet

DAC is offering complimentary wireless internet throughout the Anaheim Convention Center. Look for SSID: DAC2010.

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47 DESIGN AUTOMATION CONFERENCE

Mobile Devices

DAC has a special website built for access from handheld mobile devices. From your Windows Mobile or Blackberry device, log in to www.dac.com and you will be automatically redirected to the mobile site. Presentation schedules, the exhibitor listing and other useful information are available and optimized for viewing on small screens.

Daily Updates on DAC.com

Check the DAC website daily for a complete listing of each day's schedule, the latest exhibitor announcements, and press coverage.

Food Courts

Food courts are available in Halls B and C on the exhibit floor. Each food court includes tables with power connections for laptop plug-in.

DACnet - 2010

DACnet internet stations are available on the 2nd level by room 210A. Power outlets for laptop plug-in are also available.

Tuesday Night Party

Hilton Anaheim, Pacific Ballroom ABCD

June 15 8:00 - 11:00pm

There will be a wide array of delectable foods along with plentiful amounts of wine, beer and assorted beverages. To join these festivities, you must register as a student or full conference attendee or exhibit only. You may also register for the Guest/Family Program.

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denali

WELCOME TO ANAHEIM

WEATHER

Anaheim is one of the few places in the world with a Mediterranean climate. With 355 days of sunshine every year, it is nearly guaranteed that you willexperience a beautiful, tropical day. Anaheim offers delightful ocean breezes,

low humidity, and very little rain. The average high temperature in June is 77 degrees, cooling off at night to 59 degrees. Summer clothing is appropriate and a light jacket may be needed for the evenings.

FIRST AID ROOM

The First Aid Room is located in Lobby B of the Anaheim Convention Center. For assistance, please call ext. 8101; for an emergency call ext. 8080. A nurse will be on duty at all times while meetings and exhibits are open. Dial (714) 765-8950.

GUEST/FAMILY PROGRAM

An $80 registration fee will admit each guest or family member to the following:

1. Tuesday Night Party at the Hilton Anaheim in the Pacific Ballroom ABCD.

2. The exhibit hall (when accompanied by an attendee). Registration for the Guest/Family Program will be at the Conference Registration desk on Sunday, June 13 through Wednesday, June 16, 2010. A badge will be provided for each registered guest or family member. This badge must be worn to participate in the above activities. Children under the age of 14 are not allowed in the exhibit hall area. A $30 registration fee will allow access to the Tuesday Night Party only.

ON-SITE INFORMATION DESK

The Information Desk will be located in the Main Lobby of the Anaheim Convention Center. Dial (714) 765-2001.

ANAHEIM ATTRACTIONS

The Anaheim Resort is an 1100-acre garden district that encompasses the redesigned and expanded Anaheim Convention Center and the Disneyland Resort, which features the original Disneyland (this year is their 53rd anniversary), the thrilling new theme park – Disney's California Adventure, and the lively Downtown Disney, a new shopping, dining, and entertainment district. For more information on the Anaheim Resort and Orange County,visit www.anaheimoc.org or call the Anaheim/Orange County Visitor and Convention Bureau at (714)765-8888.

HOTEL LOCATIONS

1 - Anaheim Convention Center

2 - Hilton Anaheim Hotel

3 - Anaheim Marriott Hotel

GENERAL SESSION
BALLROOM ABC

Tuesday, June 15 8:30 - 10:15am

OPENING REMARKS

Sachin S. Sapatnekar
47th DAC General Chair

AWARDS PRESENTATIONS

KEYNOTE ADDRESS

From Contract to Collaboration: Delivering a New Approach to Foundry

Tuesday, June 15 8:30am

Douglas Grose
Chief Executive Officer, GLOBALFOUNDRIES, Sunnyvale, CA

The list of challenges facing the semiconductor industry is daunting. Chip design continues to increase in complexity, driven by product requirements that demand exponentially more performance, functionality and power efficiency, integrated into a smaller area. In parallel, manufacturing technology is facing increased challenges in materials, cost and shorter product lifecycles. This confluence of factors puts the industry at a crossroads and the foundry industry at center stage.

Chip design companies need to redefine relationships with their manufacturing partners, and foundries must create a new model that brings manufacturing and design into an integrated and collaborative process. This presentation will explore the challenges of bringing the next generation of chip innovation to market through leveraging an integrated global ecosystem of talent and technology. The world's top design companies want more than a contract manufacturer; they want a level of collaboration and flexibility supported by a robust partner ecosystem of leading providers in the EDA, IP and design services sectors.

Doug Grose is the Chief Executive Officer (CEO) of GLOBALFOUNDRIES. In this role he defines the vision and global business strategy of GLOBALFOUNDRIES as it charts new ground in leading-edge semiconductor manufacturing innovation.

Prior to joining GLOBALFOUNDRIES, Doug served as Senior Vice President of technology development, manufacturing and supply chain for Advanced Micro Devices, Inc. (AMD). In this role, he managed AMD's global manufacturing and process technology operations, including AMD fabrication facilities, AMD foundry relationships and AMD's global supply chain.

Prior to joining AMD in 2007, Grose spent 25 years at IBM as General Manager of technology development and manufacturing for the systems and technology group. Before joining IBM, Grose was an Executive Vice President and Chief Operating Officer of Nanotech Resources, Inc., a not-for-profit corporation.

Grose holds a doctoral degree in materials engineering, and a master's degree in business administration and science.

AWARDS

MARIE R. PISTILLI WOMEN IN EDA ACHIEVEMENT AWARD

Mar Hershenson - *Vice President, Product Development, Custom Design Business Unit, Magma Design Automation, Inc., San Jose, CA*

For her significant contributions in helping women advance in the field of EDA technology.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIPS FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African-American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and a volunteer committee continues to administer the program for DAC. DAC normally funds a $4000 scholarship, renewable up to five years, to graduating high school seniors.

The 2010 recipient is:

Corlan McDonald - *Attending the Univ. of Central Florida, Orlando, FL. Majoring in Computer Science.*

A. RICHARD NEWTON GRADUATE SCHOLARSHIPS

Each year the Design Automation Conference sponsors the $24,000 A. Richard Newton Graduate Scholarship to support graduate research and study in Design Automation (DA), and Design with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a University for the Faculty Investigator to expend in direct support of one or more DA graduate students. The criteria are: the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; the academic credentials of the student(s); and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Advisor: Sherief Reda - *Brown Univ., Providence, RI*

Student: **Ryan J. Cochran, Abdullah N. Nowroz** - *Brown Univ., Providence, RI*

Project: **ADAPTIVE HOT SPOT COOLING FOR MANY-CORE PROCESSORS.**

2009 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO EDA

Sponsored by the EDA Consortium and IEEE Council on EDA

Randal E. Bryant - *Dean and University Professor of the School of Computer Science at Carnegie Mellon Univ.*

Randy Bryant is the recipient of the prestigious 2009 Phil Kaufman Award for his seminal technological breakthroughs in the area of formal verification.

ACM/IEEE A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

For developing Reduced Ordered Binary Decision Diagrams forming the foundation for symbolic manipulation of logic designs with broad impacts in academia and industry.

Randal E. Bryant - *Carnegie Mellon Univ., Pittsburgh, PA*

2010 IEEE FELLOW

Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

For contributions to the design for manufacturability of integrated circuits, and the technology roadmap of semiconductors.

Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

For contributions to the design of low-power and secure systems-on-chip.

IEEE CIRCUITS AND SYSTEMS SOCIETY

2010 Pre-Doctoral Scholarship 1

Saeed Zeinolabedinzadeh Namarvar - *Univ. of Tehran, Iran*

AWARDS

IEEE CEDA DISTINGUISHED SERVICE AWARD

For distinguished service in establishing the IEEE Council on EDA.

Alfred E. Dunlop - *Crossbow Consulting, LLC, Kattskill Bay, NY*

Richard Clayton Smith - *Consultant, Prosper, TX*

Giovanni De Micheli - *EEI/CSI, EPFL, Lausanne, Switzerland*

ACM SIGDA DISTINGUISHED SERVICE AWARDS

Matthew R. Guthaus - *Univ. of California, Santa Cruz, CA*

For dedicated service as director of SIGDA CADathlon at ICCAD program (2006-2009) and Editor-in-Chief of the SIGDA eNewsletter (2007-present).

Alex K. Jones - *Univ. of Pittsburgh, Pittsburgh, PA*

For dedicated service to ACM/SIGDA and the Design Automation Conference as director of the University Booth program (2006-2009)

Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

For dedicated service as SIGDA Chair (2005-2009) and contributions to SIGDA, DAC and the EDA profession.

ACM ATHENA LECTURE AWARD

Mary Jane Irwin - *Pennsylvania State Univ., State College, PA*

For her outstanding research contributions to computer-aided design, computer arithmetic and computer architecture.

ACM OUTSTANDING PHD DISSERTATION AWARD IN ELECTRONIC DESIGN AUTOMATION

Himanshu Jain - *Carnegie Mellon Univ., Pittsburgh, PA*

For the dissertation: **VERIFICATION USING SATISFIABILITY CHECKING, PREDICATE ABSTRACTION, AND CRAIG INTERPOLATION.**

SIGDA OUTSTANDING NEW FACULTY AWARD

Deming Chen - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

Puneet Gupta - *Univ. of California, Los Angeles, Los Angeles, CA*

The SIGDA Outstanding New Faculty Award recognizes a junior faculty member early in his/her academic career who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation.

ACM TRANSACTIONS ON DESIGN AUTOMATION OF ELECTRONIC SYSTEMS (TODAES) 2010 BEST PAPER AWARD

Hao Yu - *Nanyang Technological Univ., Singapore, Singapore*

Joanna Ho - *Univ. of Notre Dame, Notre Dame, IN*

Lei He - *Univ. of California, Los Angeles, CA*

For Paper Titled: **ALLOCATING POWER GROUND VIAS IN 3-D ICS FOR SIMULTANEOUS POWER AND THERMAL INTEGRITY**
ACM TODAES 14(3) Article 41, May 2009.

The Award recognizes the best paper published in the ACM Transactions on Design Automation of Electronic Systems in the time window from April 2008 issue to January 2010 issue.

KEYNOTE SESSIONS
BALLROOM ABC

Echoes of DAC's Past: From Prediction to Realization, and Watts Next?
Wednesday, June 16 11:30am

Bernard S. Meyerson
IBM Fellow, Vice President-Innovation, IBM Corp., Yorktown Hts., NY

Over the last five years the semiconductor industry has acknowledged, but struggled to deal with, the end of classical device scaling in silicon technology. This has had ramifications across all aspects of the technology spectrum, as a steady stream of innovations, ever more fundamental, have been required to drive accustomed generational improvements in Information Technology (IT). Adding to this challenge on the demand side there has been an accelerating and seemingly insatiable need for IT resources, driven by the emergence of the 'Internet of Things'. With such heavy and growing IT demands, key metrics such as system power, cost/performance, and application specific benchmarks have become a core focus of emerging solutions. It is these same metrics and constraints that also require advances in the efficiency and optimization of IT. In this talk, I will review how our industry is dealing with each of these challenges, and explore emerging compute paradigms, such as Cloud Computing, that are impacting EDA directly.

Bernie Meyerson serves as the Vice President for Innovation, and leads IBM's Global University Relations Function within IBM's Corporate HQ organization. He is also responsible for the IBM Academy, a self-governed organization of about 1000 executives and senior technical leaders from across IBM. Meyerson was appointed to this position in October 2009.

For his innovation efforts, Meyerson was cited as "Inventor of the Year" by the New York State Legislature in 1998, and was recognized as "United States Distinguished Inventor of the Year" by the US IP Law Association and the US Patent and Trademark Office in 1999. He was most recently recognized in May of 2008 as "Inventor of the Year" by the New York State Intellectual Property Lawyers Association.

Designing the Motorola Droid
Thursday, June 17 11:15am

Iqbal Arshad
Corporate VP, Innovation Products, Motorola Mobile Devices, Inc., Libertyville, IL

As mobile internet usage skyrockets and more sophisticated mobile applications are being developed, the device formerly known as the cell phone is at a major technological inflection point. To meet this challenge, we must design devices and services that enable a transformation in the way we work, socially interact, use the web and utilize computing power. A key ingredient to making this happen is the synthesis of new hardware that is tightly coupled with a new software experience or business opportunity. Similarly, when launching new high-technology products, the success of the product largely depends on how well the target consumer is educated about the availability and capability of the new device. This talk will discuss how designing the Droid helped Motorola to address this shift in the market place.

Iqbal Arshad is Corporate Vice President of Innovation Products at Motorola Mobile Devices. He leads the team responsible for delivering all aspects of hardware and software for Motorola's breakthrough smart phone products including the latest Droid product line.

Prior to leading the product innovation group, Iqbal was vice president of Motorola's European product development and management organization. In his tenure at Motorola, Iqbal has lead development and delivery of many award winning mobile devices and mobile network products to worldwide customers. He has also held product management and development leadership positions with 3Com, and Watercove Networks.

Iqbal received his Bachelor of Science in Electrical Engineering from University of Miami, Miami, FL and Masters of Engineering Management from Northwestern University, Evanston, IL.

MANAGEMENT DAY

Tuesday, June 15 10:30am - 6:00pm

Rm: 204C

Organizer: **Yervant Zorian** - *Virage Logic Corp., Fremont, CA*

Sponsored by: cadence® Business

The DAC-2010 Management Day provides managers with timely information to help them make decisions where business and technology intersect. This is a unique opportunity for managers to gain insights from their peers in the industry.

Today's complex SOCs require different types of optimizations and the adoption of emerging solutions to meet such requirements. Optimizing for volume production, low power, and shrinking sizes necessitates accurate trade-off analysis and technical/business decision-making by management. Also, moving to new semiconductor technology nodes, such as 28nm or 40nm, can significantly affect the choices of suppliers. The Management Day sessions will discuss these changing needs and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options for flows, methodologies and suppliers.

The Management Day is comprised of three sessions. The first two sessions will feature presentations by managers representing independent device manufacturers (IDMs), fab-light ASIC providers and fabless companies. Senior managers of today's most complex nanometer chips – from CSR, Samsung, NXP, Intel, PMC Sierra, LSI Logic and other leading companies – will discuss the latest and emerging solutions, along with their economic impact. The third session will be a panel to involve the presenters and the audience in an open brainstorming discussion.

This special day provides managers with timely information to help them make decisions where business and technology intersect. This is a unique opportunity for managers to gain insights from their peers in the industry

SESSION 1 10:30am - 12:00pm

DECISION MAKING FOR COMPLEX ICs

Session Chair: **Richard Goering** - Cadence Design Systems, San Jose, CA

Moving to new semiconductor technology nodes for complex ICs can significantly affect the choices of design flow, methodologies and suppliers. The session will cover the challenges of complex chip design and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options. This session feature presentations by managers representing independent device manufacturers (IDMs), fab-light ASIC providers, and fabless companies.

Speakers:
Ken Wagner - *Vice President of Engineering, PMC-Sierra, Inc., Kanata, ON, Canada*
Ty Garibay - *Senior Director, OMAP IC Design, Texas Instruments, Inc., Austin, TX*
Jitu Khare - *Director of Central Engineering, Applied Micro Circuits Corp.*

SESSION 2 2:00 - 4:00pm

TRADE-OFFS AND CHOICES FOR EMERGING SOCs

Session Chair: **Gary Smith** - *GarySmith EDA, Santa Clara, CA*

Today's emerging SOCs require multiple types of optimizations and the adoption of advanced solutions to meet stringent design requirements.

Optimizing for volume production, low power, and shrinking sizes necessitates accurate trade-off analysis and technical/business decision-making by management. This session will feature senior managers of today's most complex nanometer chips

Speakers:
Mark Redford - Vice President, Advanced Process Technology Development, *CSR, San Jose, CA*
Robert Madge - *Director of Technology, and Prabhu Krishnamurthy, Director of Design Tools and Methodology, LSI Logic Corp., Milpitas, CA*
Michael Jassowski, *Business & Technology Programs, Intel Corp.*
Barry Dennington - Senior Vice President, *NXP Semiconductors, Southampton, United Kingdom*
Karim Arabi - *Director, Qualcomm, Inc.*

SESSION 3 4:30 - 5:30pm

MAKING CRITICAL DECISIONS FOR EMERGING SOC DEVELOPMENT

Session Moderator: **Ron Wilson** - *Reed Business,San Jose, CA*

Panelists: The speakers from Sessions 1 and 2

The panel complements the two management presentation sessions (numbers) where the key managers of today's most complex nanometer chips will discuss the emerging solutions and discuss their economic impact. This Management Day panel will provide a unique opportunity for all attending managers to interact directly with the panelists and gain insights from their peers in the industry.

Speakers:
Mark Redford - Vice President, Advanced Process Technology Development, *CSR, San Jose, CA*
Ken Wagner - *PMC-Sierra, Inc. Kanata, ON, Canada*
Karim Arabi - *Qualcom, Inc., San Diego, CA*
Ty Garibay - *Texas Instruments, Inc., Austin, TX*
Robert Madge - *LSI Logic Corp., Milpitas, CA*
Jitu Khare - *Applied Micro Circuits Corp., Sunnyvale, CA*

EMBEDDED/SOC ENABLEMENT DAY

Thursday, June 17 9:00am - 6:00pm

Rm: 303A

Organizer: **Yervant Zorian** - *Virage Logic Corp., Fremont, CA*

The embedded processor System-On-Chip market is being hotly contested right now as companies vie for their piece of this high stakes segment of the semiconductor industry. IC design engineers, embedded systems designers, IP integrators, FPGA designers, investors, foundry reps and the media will be on hand in this new forum to hear from market leaders and network with each other. The Embedded/SOC Enablement Day is a day-long track of sessions dedicated to bringing industry stakeholders together in one room to shed light on where SOC design is headed. The day is comprised of presentations from leading SOC enabling sectors including embedded processors, embedded systems, EDA, FPGA, IP, foundry, and design services.

Presenters will focus on optimization of embedded and application-domain specific operating systems, system architecture for future SOCs, application-specific architectures based on embedded processors and technical/business decision making by program developers. They will cover the state-of-the-art in enablement solution for embedded systems and complex SOCs. Such solutions often require tight collaboration between diverse players in this eco-system. Moving to new embedded SOC technology nodes can significantly affect the choices of suppliers. The new Embedded/SOC Enablement Day provides a unique opportunity to foster discussions that address all aspects of the SOC development ecosystem.

The Embedded / SOC Enablement Day is a day-long track dedicated to bringing industry stakeholders together in one room to shed light on where embedded SOC design is headed. SOC design engineers, embedded systems designers, IP integrators, FPGA designers, investors, foundry representatives and the analysts will be on hand in this new forum to hear from industry leaders and network with each other. Each session will be comprised of four presentations followed by a discussion panel, where key senior managers of today's design ecosystem will discuss the emerging trends and share their vision.

SESSION 1 9:00 - 11:00am

ENABLING TOMORROW'S COMPLEX SOCs

Session Chair: **Peggy Aycinena** - *EDA Confidential- San Mateo, CA*

Invited Keynote:
Gadi Singer - *Vice President & General Manager, SoC Enabling Group, Intel- Santa Clara, CA*

Presenters:
Sami Issa - *Executive Director, Advanced Technology Investment Company (ATIC)*
Alex Shubat - *President & Chief Executive Officer, Virage Logic, Fremont, CA*
John Bruggeman - *Chief Marketing Officer, Cadence Design Systems, San Jose, CA*

The embedded processor based System-on-Chip market is being hotly contested right now as companies vie for their piece of this high stakes segment of the semiconductor industry. This session is comprised of presentations from leading SOC enabling sectors including embedded processors, semiconductor investments, IP and EDA providers

SESSION 2 2:00 - 4:00pm

TRADE-OFFS AND CHOICES FOR EMEBEDDED SOLUTIONS

Session Chair: **Nic Mokhoff** - *EE Times / Techinsights, Manhasset, NY*

Presenters:
James Ready - *Chief Technology Officer, MontaVista Software, Santa Clara, CA*
Ivo Bolsens - *CTO & Senior Vice President, Xilinx, San Jose, CA*
Shauh-Teh Juang - *Senior Director, Design & Technology Platform, TSMC, San Jose, CA*
John Goodenough - *Director of Design Technology, ARM, Sheffield, GB*

Moving to new embedded SOC solutions can significantly affect the choices of suppliers. This session provides a unique opportunity to foster discussions that address different aspects of the SOC development trade-offs.

SESSION 3 4:30 - 6:00pm

LEVERAGING A DIVERSE DESIGN ECO-SYSTEM FOR EMERGING SOC DEVELOPMENT

Session Moderator: Lucio Lanza, Lanza Tech Ventures, Palo Alto, CA

Presenters:
Naveed Sherwani - *President & CEO, Open Silicon, Milpitas, CA*
Glenn Perry - *General Manager, Embedded Software Division, Mentor Graphics*
Mark Dickenson - *VP of Systems Solutions, Altera*

This session will cover the state-of-the-art in enablement solution for embedded systems and complex SoCs. Such solutions often require tight collaboration between diverse players in this design eco-system.

TECHNICAL PROGRAM HIGHLIGHTS

The technical program for DAC 2010 has an exceptional quality of technical papers, panels, special sessions, WACI (Wild and Crazy Ideas), full day tutorials and User Track. The program is tailored for researchers and developers in the electronic design and automation (EDA) industry, design engineers, and management. It highlights the advancements and emerging trends in the design of electronic circuits and systems.

The core of the technical program consists of 148 peer-reviewed papers selected from 607 submissions (24% acceptance ratio). Organized in the 35 technical paper sessions, these papers cover a broad set of topics ranging from system-level design, low-power, physical design and manufacturing, embedded systems, logic and high level synthesis, simulation, verification, test, and emerging technologies. Popular submission themes were:

1. Power analysis and low-power (83 submissions, 5 sessions)
2. Physical Design and Manufacturability (72 submissions, 4 sessions)
3. System-Level Design and Analysis (69 submissions, 4 sessions)

Some of the novel papers present cutting research in property checking, global routing, variation characterization, silicon mismatch, cache design for routers, rewiring, logic optimization with don't cares, Boolean matching, and low energy processor design. The submissions indicate the increasing importance of system level design, low-power design and analysis, and physical design and manufacturability.

Special sessions will deal with a wide variety of themes such as progress in networks-on-chip research, virtualization for mobile embedded devices, challenges in analog modeling, introduction to cyber-physical systems, design for reliability, designing resilient systems from unreliable components, a holistic view on energy management – cell phones to power grids and post-silicon validation. Leading research and industry experts will present their views on these topics.

Embedded/SOC Enablement Day is designed to further advance DAC's partner eco-system and build long-term relationships with mutual customers. The day is comprised of representatives from leading SOC enabling sectors including embedded processors, FPGA, embedded systems, EDA, IP, foundry, and design services. Presenters will focus on the state-of-the-art in enablement solution for embedded systems and complex SOCs. Such solutions often require tight collaboration between diverse players in this eco-system. As we move to higher levels of embedded SOC complexity, these collaborative solutions will significantly affect the choices of suppliers. This new Embedded/SOC Enablement Day provides a unique opportunity to foster knowledge dissemination and open discussions that address all aspects of the SOC development ecosystem.

The User Track at DAC is in its second year. It highlights contributions by users of EDA flows and tools, and targets designers and practitioners: design tool users, hardware or software designers, application engineers, consultants, and flow or methodology developers. This year, we received 149 submissions, a 27% increase from last year's submissions. The reviewing committee consisted of experienced tool users from various companies. The User Track program presents eight paper sessions, three poster sessions, and a panel. The panel sessions allow a unique opportunity to interact with presenters and other DAC attendees. The topics span both front-end and back-end sessions, and highlight several challenges, solutions and methodologies covering verification, timing analysis, ASIC, and FPGA design flows, IP block integration, and test and debug.

This year's DAC panels cover nearly every aspect of the design flow. The panel sessions start off with a look to the future by a wide range of leaders from the semiconductor industry. The other seven panels have something for everyone. Panels will explore the future of TSV/3-D technology, the current state of high level synthesis, different approaches to addressing process variability, the future of low-power design methodologies and how to bridge pre-silicon verification/post-silicon validation. Panels will also take a look at what is needed for an always connected car. Finally, if you've wondered what cloud computing is all about, a panel will explore how cloud computing fits in with the EDA industry.

The program includes six tutorials on timely subjects, including four design topics: 3-D integrated circuits, analog mixed-signal design, system-level design, and low-power design. This year also features tutorials on two special topics. The first is an overview of software engineering that includes introductions to agile, lean, scrum, and other software best practices—topics that will offer immediate and practical value to students, EDA developers, and SOC firmware engineers. The second is a tutorial on the importance of effective marketing and should appeal to a broad range of DAC attendees that wish to better understand this aspect of business success. As in the past, the goal of the DAC tutorials is to provide practical, useable, and up-to-date knowledge that attendees can immediately apply in their jobs or studies.

TECHNICAL SESSIONS

Tuesday, June 15 10:30am - 12:00pm

1 PANEL: EDA CHALLENGES AND OPTIONS: INVESTING FOR THE FUTURE

Rm: 207AB

General Interest

Chair: **William Joyner** - *Semiconductor Research Corp., Research Triangle Pk., NC*
Organizer: **Ruchir Puri** - *IBM Corp., Yorktown Hts., NY*

As the overall economy and the semiconductor industry emerges from one of the worst recessions in years, it is time to take stock of the challenges that face the EDA industry in the coming years. Like many other parts of the economy, the semiconductor industry faces a cost crunch that heralds a new era of financial restraint. Add to this the complexities of future technology nodes at 32nm and beyond, and there is a heady mix of technology complexity and unprecedented productivity requirements on future design flows. This confluence presents a significant opportunity as well as a complex challenge for the EDA industry. It is crucial for the IC design and CAD community to comprehend the issues that underlie the demands of this new world. This panel brings together representatives of major EDA stakeholders, i.e., customers, EDA companies, technology providers, and the research community, as they determine which of these challenges will dominate the field in the near- and long-term future, and which can be sold short.

Speakers:
Raj Jammy - *SEMATECH, Austin, TX*
Ahmed Jerraya - *CEA-LETI MINATEC, Grenoble, France*
Jan Rabaey - *The Multi Scale Systems Center and Univ. of California, Berkeley, CA*
Wally Rhines - *EDA Consortium & Mentor Graphic Corp., Wilsonville, OR*
Leon Stok - *IEEE CEDA Design Technology Council & IBM Corp., Hopewell Jct., NY*

2 SPECIAL SESSION: POST-SILICON VALIDATION OR AVOIDING THE $50 MILLION PAPERWEIGHT

Rm: 209AB

Verification and Test

Chair: **David Lackey** - *IBM Corp., Essex Junction, VT*
Organizer: **Nicola Nicolici** - *McMaster Univ., Hamilton, ON, Canada*

Pre-silicon verification methods work with models of the design and are therefore limited by the inherent trade-off between accuracy and run-time. Designs are sent to fabrication when the confidence level is sufficiently high; design errors, be they functional or electrical bugs, slip through to fabrication and need to be detected on the silicon prototypes. Therefore, the pre-silicon verification transitions to post-silicon validation upon return of first silicon samples from the fab. Increasing the productivity by tackling post-silicon validation in a structured manner is becoming essential to reduce the number of silicon spins and, more importantly, product recalls with potentially catastrophic consequences. This special session describes opportunities for EDA and academia to help with this problem, indicates the role of validation, and outlines recent advances in tacking this problem.

2.1 POST-SILICON VALIDATION CHALLENGES: HOW EDA AND ACADEMIA CAN HELP
Jagannath Keshava, Nagib Hakim - *Intel Corp., Santa Clara, CA*
Chinna Prudvi - *Intel Corp., Hillsboro, OR*

2.2 POST-SILICON IS TOO LATE - AVOIDING THE $50 MILLION PAPERWEIGHT STARTS WITH VALIDATED DESIGNS
John Goodenough, Rob Aitken - *ARM Ltd., San Jose, CA*

2.3 POST-SILICON VALIDATION: OPPORTUNITES, CHALLENGES AND RECENT ADVANCES
Subhasish Mitra - *Stanford Univ., Stanford, CA*
Sanjit A. Seshia - *Univ. of California, Berkeley, CA*
Nicola Nicolici - *McMaster Univ., Hamilton, ON, Canada*

3 SPEED UP YOUR MODEL! RTL, DATA-FLOW, OR SYSTEMC

Rm: 207D

System-Level and Embedded

Chair: **Luciano Lavagno** - *Politecnico di Torino, Torino, Italy*

This session presents approaches to speed up execution of models used in system-level design. The first paper proposes a data-flow model for LTE physical layer of 4G mobile wireless networks, which identifies clusters to apply static scheduling and improves the run time execution. The second paper abstracts RTL to C++ code to match the simulation speed required for embedded software development by capturing the functionality without the implementation details. The third paper applies a dynamic scheduling technique in FPGA processing in order to emulate SystemC programs efficiently.

3.1 A MIXED-MODE VECTOR-BASED DATA-FLOW APPROACH FOR MODELING AND SIMULATING LTE PHYSICAL LAYER
Chia-Jui Hsu, José Luis Pino - *Agilent, Westlake Village, CA*
Fei-Jiang Hu - *Agilent, Beijing, China*

3.2 ABSTRACTION OF RTL IPS INTO EMBEDDED SOFTWARE
Nicola Bombieri, **Franco Fummi**, Graziano Pravadelli - *Univ. di Verona, Verona, Italy*

3.3 ONLINE SYSTEMC EMULATION ACCELERATION
Scott S. Sirowy, Chen Huang, Frank Vahid - *Univ. of California, Riverside, CA*

TECHNICAL SESSIONS

Tuesday, June 15 10:30am - 12:00pm

4 EMBEDDED SOFTWARE TIMING MATTERS!

Rm: 207C

System-Level and Embedded

Chair: **Eli Bozorgzadeh** - *Univ. of California, Irvine, CA*

Software execution time is one of the most important issues in embedded system design and takes different forms that depend on the application context. The first paper presents a method to optimize both latency and throughput of packet-processing systems in a soft real-time context. Focusing on hard real-time systems, the second paper discusses a scheduling approach to optimize energy efficiency. How to estimate the worst-case execution time of Esterel programs for multiprocessors is the subject of the third paper. The session is concluded by a paper that presents an efficient implementation of breadth-first search on Graphics Processing Unit (GPU).

4.1 LATA: A LATENCY AND THROUGHPUT-AWARE PACKET PROCESSING SYSTEM
Jilong Kuang, Laxmi Bhuyan - *Univ. of California, Riverside, CA*

4.2 A PROBABILISTIC AND ENERGY-EFFICIENT SCHEDULING APPROACH FOR ONLINE APPLICATION IN REAL-TIME SYSTEMS
Thorsten Zitterell, Christoph Scholl - *Univ. Freiburg, Freiburg, Germany*

4.3S TIMING ANALYSIS OF ESTEREL PROGRAMS ON GENERAL-PURPOSE MULTIPROCESSORS
Lei Ju, Bach Khoa Huynh, Abhik Roychoudhury - *National Univ. of Singapore, Singapore*
Samarjit Chakraborty - *Technische Univ. München, Germany*

4.4S AN EFFECTIVE GPU IMPLEMENTATION OF BREADTH-FIRST SEARCH
Lijuan Luo, Martin D.F. Wong, Wen-Mei Hwu - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

5 THERMAL TRACKING, MONITORING AND CHARACTERIZATION

Rm: 210AB

Low-Power Design

Chair: **Seda Ogrenci Memik** - *Northwestern Univ., Evanston, IL*

Thermal phenomena have become a first order concern for computer systems. The papers in this session focus on three problems in this area. The first paper described techniques to track temperature changes for high performance systems. The second paper investigates predicting and controlling thermals at run-time through phase detection. The last paper focuses on optimally allocating thermal sensors for accurate full thermal characterization.

5.1 THERMAL MONITORING OF REAL PROCESSORS: TECHNIQUES FOR SENSOR ALLOCATION AND FULL CHARACTERIZATION
Abdullah N. Nowroz, Ryan J. Cochran, Sherief Reda - *Brown Univ., Providence, RI*

5.2 CONSISTENT RUN-TIME THERMAL PREDICTION AND CONTROL THROUGH WORKLOAD PHASE DETECTION
Ryan J. Cochran, Sherief Reda - *Brown Univ., Providence, RI*

5.3 ADAPTIVE AND AUTONOMOUS THERMAL TRACKING FOR HIGH PERFORMANCE COMPUTING SYSTEMS
Yufu Zhang, Ankur Srivastava - *Univ. of Maryland, College Park, MD*

6 ADVANCED CLOCK DESIGN AND FLIP-CHIP LAYOUT

Rm: 210CD

Physical Design

Chair: **Yegna Parasuram** - *Mentor Graphics Corp., San Jose, CA*

This session focuses on the efficient construction of high-performance clocks, as well as on flip-chip routing. The first paper presents techniques to optimize wires and buffers in non-uniform clock meshes. The second paper demonstrates a SPICE-validated technique for the ultra-fast construction of clock trees. The third paper exploits a novel delay modeling technique for clock-tree design. The final paper in this session describes a fast flip-chip routing algorithm.

6.1 NON-UNIFORM CLOCK MESH OPTIMIZATION WITH LINEAR PROGRAMMING BUFFER INSERTION
Matthew Guthaus - *Univ. of California, Santa Cruz, CA*
Gustavo Wilke, Ricardo Reis - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

6.2 FAST TIMING-MODEL INDEPENDENT BUFFERED CLOCK-TREE SYNTHESIS
Xin-Wei Shih, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

6.3S CLOCK-TREE SYNTHESIS UNDER AGGRESSIVE BUFFER INSERTION
Ying-Yu Chen, Chen Dong, Deming Chen - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

6.4S GLOBAL ROUTING AND TRACK ASSIGNMENT FOR FLIP-CHIP DESIGNS
Xiaodong Liu, Jian Sun, Xuan Zeng - *Fudan Univ., Shanghai, China*
Yifan Zhang, Chunlei Zhu - *Synopsys, Inc., Shanghai, China*
Gary Yeap - *Synopsys, Inc., Mountain View, CA*

TECHNICAL SESSIONS

Tuesday, June 15 2:00 - 4:00pm

7 Rm: 207AB PANEL: BRIDGING PRE-SILICON VERIFICATION AND POST-SILICON VALIDATION

Verification and Test

Chair: **Alan Hu** - *Univ. of British Columbia, Vancouver, BC, Canada*
Organizers: **Rajesh Galivanche** - *Intel Corp., Santa Clara, CA*
Amir Nahir - *IBM Corp., Haifa, Israel*
Avi Ziv - *IBM Corp., Haifa, Israel*

Speakers:
Miron Abramovici - *Tiger's Lair, Inc., Vienna, VA*
Bob Bentley - *Intel Corp., Hillsboro, OR*
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*
Albert Camilleri - *Qualcomm, Inc., San Diego, CA*
Harry Foster - *Mentor Graphics Corp., Plano, TX*
Shakti Kapoor - *IBM Corp., Austin, TX*

As much as designers strive to fully validate their design before committing to silicon, post-silicon validation is a necessary step in a design's verification process. Pre-silicon techniques such as simulation and emulation are naturally limited in scope and volume as compared to what can be achieved on the silicon itself. Some parts of the verification, such as full-system functional verification, cannot be practically covered with current pre-silicon technologies. Also, post-silicon validation engineers are typically not designers or architects, and much of the knowledge that goes into developing pre-silicon verification collateral is not leveraged for post-silicon validation, but instead is developed all over again.

In this panel, experts from industry, academia, and EDA will examine the differences and similarities between pre- and post-silicon. The discussion will focus on how the fundamental aspects of verification are affected by these differences and explore how the gaps between the two worlds can be bridged.

8 Rm: 209AB SPECIAL SESSION: VIRTUALIZATION IN THE EMBEDDED SYSTEMS: WHERE DO WE GO?

System-Level and Embedded

Chair: **Alasdair Rawsthorne** - *The Univ. of Manchester, United Kingdom*
Organizer: **Bjorn De Sutter** - *Ghent Univ., Ghent, Belgium*

Both system virtualization (such as VMWare, Xen, etc.) and process virtualization (Java, .NET, Flash) are very mature technologies in the server and desktop market. On contemporary heterogeneous multicore embedded platforms that typically feature programmable accelerators, virtualization is still an emerging technology. Many people agree that virtualization can play a central role in meeting many of the constraints of embedded systems with respect to power efficiency (hardware consolidation in heterogeneous multicores), security and safety (isolating software domains that were isolated physically before), and reliability. At the same time, virtualization will offer a perspective of homogeneity to programmers, thus increasing their productivity. Finally, virtualization accelerators will likely ease the integration of different components, thus facilitating hardware reuse and a horizontal market. However, there are still many challenges left to be solved, as outlined in this special session.

8.1 COMPILATION AND VIRTUALIZATION IN THE HIPEAC VISION
Christian Bertin, Christophe Guillon - *STMicroelectronics, Grenoble, France*
Koen De Bosschere - *Ghent Univ., Ghent, Belgium*

8.2 PROCESSOR VIRTUALIZATION AND SPLIT COMPILATION FOR HETEROGENEOUS MULTICORE EMBEDDED SYSTEMS
Albert Cohen - *INRIA, Orsay, France*
Erven Rohou - *INRIA, Rennes, France*

8.3 FINE-GRAINED I/O ACCESS CONTROL BASED ON XEN VIRTUALIZATION FOR 3G/4G MOBILE DEVICES
Jong-Deok Choi, Sung-Min Lee, **Sang-Bum Suh** - *Samsung, Suwon, Republic of Korea*

8.4 DEVICE HYPERVISORS
Johan Fornaeus - *Wind River Systems, Inc., Alameda, CA*

9 Rm: 207D MEMORY AND MULTIPROCESSOR DESIGN SPACE EXPLORATION

System-Level and Embedded

Chair: **Ann Gordon-Ross** - *Univ. of Florida, Gainesville, FL*

This session focuses on system-level exploration of memory and multiprocessor architectures. The first paper presents a novel correlation-based technique to predict expected improvement of multiprocessor configurations in order to speed up exploration. The second paper introduces models for estimating various costs during exploration of 3-D many-core systems. The third paper proposes cache partitioning techniques for a multicore system to reduce off-chip memory bandwidth requirements. The fourth paper describes an approach for exploring SRAM designs by generating optimized virtual prototypes that can be readily refined for further exploration.

9.1 A CORRELATION-BASED DESIGN SPACE EXPLORATION METHODOLOGY FOR MULTIPROCESSOR SYSTEMS-ON-CHIP
Aleksandar Brankovic, Jovana Jovic, **Giovanni Mariani** - *ALaRI, Univ. of Lugano, Switzerland*
Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, - *Politecnico di Milano, Milan, Italy*

9.2 COST-AWARE THREE-DIMENSIONAL (3-D) MANY-CORE MULTIPROCESSOR DESIGN
Jishen Zhao, Xiangyu Dong, Yuan Xie - *Pennsylvania State Univ., University Park, PA*

9.3 OFF-CHIP MEMORY BANDWIDTH MINIMIZATION THROUGH CACHE PARTITIONING FOR MULTICORE PLATFORMS
Chenjie Yu, Peter Petrov - *Univ. of Maryland, College Park, MD*

9.4 VIRTUAL PROTOTYPER (VIPRO): AN EARLY DESIGN SPACE EXPLORATION AND OPTIMIZATION TOOL FOR SRAM DESIGNERS
Satyanand Nalam, Benton H. Calhoun - *Univ. of Virginia, Charlottesville, VA*
Mudit Bhargava, Ken Mai - *Carnegie Mellon Univ., Pittsburgh, PA*

TECHNICAL SESSIONS

Tuesday, June 15 2:00 - 4:00pm

10 INTERCONNECT NETWORKS: PRESENT AND FUTURE

Rm: 207C

System-Level and Embedded

Chair: **Li Shang** - *Univ. of Colorado, Boulder, CO*

This session presents leading research in interconnect networks. The first two papers comprehensively examine interconnection networks in 3-D. The third paper describes a many-core system with nano-photonic interconnect. The last two papers describe traditional interconnect architectures: the fourth paper compares virtual channels with multiple physical networks; and the final paper explains an efficient dynamic reconfigurable on-chip network architecture.

10.1 QUANTIFYING AND COPING WITH PARAMETRIC VARIATIONS IN 3-D-STACKED MICROARCHITECTURES
Serkan Ozdemir - *Univ. Politècnica de Catalunya, Barcelona, Spain*
Yan Pan, Abhishek Das, Gokhan Memik - *Northwestern Univ., Evanston, IL*
Gabriel Loh - *Georgia Institute of Technology, Atlanta, GA*
Alok Choudhary - *Northwestern Univ., Evanston, IL*

10.2 COST-DRIVEN 3-D INTEGRATION WITH INTERCONNECT LAYERS
Xiaoxia Wu, Guangyu Sun, Xiangyu Dong, Reetuparna Das, Yuan Xie, Chita Das - *Pennsylvania State Univ., State College, PA*
Jian Li - *IBM Corp., Austin, TX*

10.3 A MULTILAYER NANOPHOTONIC INTERCONNECTION NETWORK FOR ON-CHIP MANY-CORE COMMUNICATIONS
Xiang Zhang, **Ahmed Louri** - *Univ. of Arizona, Tucson, AZ*

10.4S VIRTUAL CHANNELS VS. MULTIPLE PHYSICAL NETWORKS: A COMPARATIVE ANALYSIS
Young Jin Yoon, Nicola Concer, Michele Petracca, Luca Carloni - *Columbia Univ., New York, NY*

10.5S AN EFFICIENT DYNAMICALLY RECONFIGURABLE ON-CHIP NETWORK ARCHITECTURE
Mehdi Modarressi, Hamid Sarbazi-Azad - *Sharif Univ. of Technology, Tehran, Iran*
Arash Tavakkol - *Institute for Research in Fundamental Sciences, Tehran, Iran*

11 CORE TECHNIQUES IN FORMAL VERIFICATION

Rm: 210AB

Verification and Test

Chair: **Pranav Ashar** - *Real Intent, Inc., Sunnyvale, CA*

This session covers recent advances in core verification techniques. The first paper presents a framework for quantified Boolean formulas. The second paper focuses on property checking. The third paper identifies parts of a netlist that are covered by a property. The last paper introduces a new algorithm to verify generalized false paths.

11.1 AN AIG-BASED QBF-SOLVER USING SAT FOR PREPROCESSING
Florian Pigorsch, Christoph Scholl - *Univ. Freiburg, Freiburg, Germany*

⏩11.2 ANALYZING K-STEP INDUCTION TO COMPUTE INVARIANTS FOR SAT-BASED PROPERTY CHECKING
Max Thalmaier, Minh Nguyen, Markus Wedler, Dominik Stoffel - *Technische Univ. Kaiserslautern, Germany*
Jörg Bormann - *Abstract RT Solutions GmbH, Munich, Germany*
Wolfgang Kunz - *Technische Univ. Kaiserslautern, Germany*

11.3 COVERAGE IN INTERPOLATION-BASED MODEL CHECKING
Hana Chockler - *IBM Corp., Haifa, Israel*
Daniel Kroening - *Oxford Univ., United Kingdom*
Mitra Purandare - *ETH Zürich, Zurich, Switzerland*

11.4 AN EFFICIENT ALGORITHM TO VERIFY GENERALIZED FALSE PATHS
Olivier R. Coudert - *OC Consulting, Holzkirchen, Germany*

12 NEW FRONTIERS IN ROUTING

Rm: 210CD

Physical Design

Chair: **Minsik Cho** - *IBM Corp., Yorktown Hts., NY*

This session advances the state-of-the-art in routing through novel multithreading and combinatorial techniques. The first paper overcomes the run-time limitations of ILP-based global routing through novel parallelization algorithms. The second paper proposes a new collision-aware concurrency strategy for multithreaded global routing. The third paper adapts a hierarchical bubble sort algorithm to untangle buses for planar PCB routing. The last paper solves the PCB bus escape routing problem using an optimal combinatorial formulation.

⏩12.1 A PARALLEL INTEGER PROGRAMMING APPROACH TO GLOBAL ROUTING
Tai-Hsuan Wu, **Azadeh Davoodi**, Jeffrey Linderoth - *Univ. of Wisconsin, Madison, WI*

12.2 MULTITHREADED COLLISION-AWARE GLOBAL ROUTING WITH BOUNDED-LENGTH MAZE ROUTING
Wen-Hao Liu, Wei-Chun Kao, Yih-Lang Li - *National Chiao Tung Univ., Hsinchu, Taiwan*
Kai-Yuan Chao - *Intel Corp., Hillsboro, OR*

12.3 TWO-SIDED SINGLE-DETOUR UNTANGLING FOR BUS ROUTING
Jin-Tai Yan, **Zhi-Wei Chen** - *Chung Hua Univ., Hsinchu, Taiwan*

12.4 AN OPTIMAL ALGORITHM FOR FINDING DISJOINT RECTANGLES AND ITS APPLICATION TO PCB ROUTING
Hui Kong, Qiang Ma, Tan Yan, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

TECHNICAL SESSIONS

Tuesday, June 15 4:30 - 6:00pm

13 PANEL: WHO SOLVES THE VARIABILITY PROBLEM?

Rm: 207AB

Physical Design

Chair: **Jamil Kawa** - *Synopsys, Inc., Mountain View, CA*
Organizers: **Nagaraj NS** - *Texas Instruments, Inc., Dallas, TX*
Juan Rey - *Mentor Graphics Corp., San Jose, CA*

Speakers:
Rob Aitken - *ARM Ltd., San Jose, CA*
Christian Lütkemeyer - *Broadcom Corp., Irvine, CA*
Vijay Pitchumani - *Intel Corp., Santa Clara, CA*
Andrzej Strojwas - *Carnegie Mellon Univ., Pittsburgh, PA*
Steve Trimberger - *Xilinx, Inc., San Jose, CA*

Though innovations in manufacturing technology help in reducing variations, they are a fact of life in IC design. In addition to random variations, systematic stress induced variations are becoming increasingly important. This panel will bring the diverse views from academia, foundries, fabless design companies, and IDM communities to address next generation solutions to variability, emphasizing design and architecture solutions. Specifically, this panel will discuss:

- Could new architectures mitigate variability in 22nm and beyond?
- Could design regularity effectively mitigate variability?
- What design techniques could be used to minimize variability 'on-the-fly'?
- What new techniques could be used for memories, register arrays and flip-flops?

14 SPECIAL SESSION: JOINT DAC/IWBDA SPECIAL SESSION - ENGINEERING BIOLOGY: FUNDAMENTALS AND APPLICATIONS

Rm: 209AB

General Interest

Chair: **Ron Weiss** - *Massachusetts Institute of Technology, Cambridge, MA*
Organizers: **Marc Reidel** - *Univ. of Minnesota, Minneapolis, MN*
Soha Hassoun - *Tufts Univ., Medford, MA*

Synthetic Biology has emerged as a powerful field with applications encompassing health care, chemical and materials production, and energy. This session emphasizes fundamental engineering principles underlying the engineering of biology. Pam Silver will describe designing and constructing proteins and cells with predictable biological properties that serve as potential therapeutics, cell-based sensors and factories for generating bio-energy, high value commodities and bio-remediation. J. Christopher Anderson will demonstrate how complex biological functions can be decomposed into modular devices for the construction of therapeutic organisms and new tools for building complex systems. Richard Murray will discuss the use of concepts from control and dynamical systems in the analysis and design of biological feedback circuits at the molecular level.

14.1 DESIGNING BIOLOGICAL SYSTEMS
Pamela Silver - *Harvard Univ., Cambridge, MA*

14.2 PROGRAMMING CELLS AS THERAPEUTICS BY MODULAR DESIGN
J. Christopher Anderson - *Univ. of California, Berkeley, CA*

14.3 WHY HUMAN-DESIGNED BIOLOGICAL CIRCUITS STINK (AND WHAT WE SHOULD DO ABOUT IT)
Richard Murray - *California Institute of Technology, Pasadena, CA*

15 RELIABILITY AND INTEGRITY OF CIRCUITS AND SYSTEMS

Rm: 207D

System-Level and Embedded

Chair: **Sudeep Pasricha** - *Colorado State Univ., Ft. Collins, CO*

This session focuses on novel methods for ensuring reliability and integrity of circuits and systems. The first paper develops a new thermal testing for ensuring post-silicon circuit integrity by detecting possible Trojans. The second paper introduces a new error injection tool for verifying system-level integrity. The last paper presents a new system-level reliability analysis by developing early quantification techniques and SAT-assisted simulations to control BDD size.

15.1 GATE-LEVEL CHARACTERIZATION: FOUNDATIONS AND HARDWARE SECURITY APPLICATIONS
Sheng Wei, **Saro Meguerdichian**, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

15.2 SCEMIT: A SYSTEMC ERROR AND MUTATION INJECTION TOOL
Peter Lisherness, Kwang-Ting Cheng - *Univ. of California, Santa Barbara, CA*

15.3 TOWARDS SCALABLE SYSTEM-LEVEL RELIABILITY ANALYSIS
Michael Glaß, Martin Lukasiewycz, Christian Haubelt, Jürgen Teich - *Univ. Erlangen-Nürnberg, Erlangen, Germany*

TECHNICAL SESSIONS

Tuesday, June 15 4:30 - 6:00pm

16 EMBEDDED HARDWARE FOR SECURITY, DATA TYPE REFINEMENT, AND ARBITRATION

Rm: 207C

System-Level and Embedded

Chair: **Sanghamitra Roy** - *Utah State Univ., Logan, UT*

This session presents innovative hardware design techniques in three areas. The first two papers describe design techniques for secure embedded hardware modules. The next two papers present novel approaches to finite precision refinement. The final paper presents a modeling technique for arbitration units. Together, these papers describe novel hardware design for addressing critical issues in embedded systems.

16.1S QUALITY METRIC EVALUATION OF A PHYSICAL UNCLONABLE FUNCTION DERIVED FROM AN IC'S POWER DISTRIBUTION SYSTEM
Ryan Helinski, James F. Plusquellic - *Univ. of New Mexico, Albuquerque, NM*
Dhruva Acharyya - *Verigy Ltd., Cupertino, CA*

16.2S THEORETICAL ANALYSIS OF GATE-LEVEL INFORMATION FLOW TRACKING
Jason Oberg, Ali U. Irturk, Ryan Kastner - *Univ. of California at San Diego, La Jolla, CA*
Wei Hu - *Northwestern Polytechnical Univ., Xian, China*
Mohit Tiwari, Timothy Sherwood - *Univ. of California, Santa Barbara, CA*

16.3 EXPLOITING FINITE PRECISION TO GUIDE DATA FLOW MAPPING
David Novo, Min Li, Robert Fasthuber, Praveen Raghavan, Francky Catthoor - *IMEC, Leuven, Belgium*

16.4S ROBUST DESIGN METHODS FOR HARDWARE ACCELERATORS FOR ITERATIVE ALGORITHMS IN SCIENTIFIC COMPUTING
Adam B. Kinsman, Nicola Nicolici - *McMaster Univ., Hamilton, ON, Canada*

16.5S NEW MODEL-DRIVEN DESIGN AND GENERATION OF MULTI-FACET ARBITERS PART I: FROM THE DESIGN MODEL TO THE ARCHITECTURE MODEL
Jer Min Jou, Sih-Sian Wu, **Yun-Lung Lee**, Cheng Chou - *National Cheng Kung Univ., Tainan, Taiwan*
Yuan-Long Jeang - *Kun Shan Univ., Tainan,Taiwan*

17 STATISTICAL TECHNIQUES FOR SILICON-TO-MODEL CORRELATION

Rm: 210AB

Verification and Test

Chair: **Chandu Visweswariah** - *IBM Corp., Hopewell Jct., NY*

In this session, the authors present three papers on the latest technical advances in this area. The first paper introduces a brand new technique, Bayesian Virtual Probe, to efficiently characterize the spatial correlation of process variation. The second paper is a significant improvement for worst case corner speedpath identification with consideration of pre-silicon modeling error. The third paper proposes a novel formulation for identifying failing segments on speedpaths, making one more step forward in the pursuit of post-silicon verification.

⏩17.1 BAYESIAN VIRTUAL PROBE: MINIMIZING VARIATION CHARACTERIZATION COST FOR NANOSCALE IC TECHNOLOGIES VIA BAYESIAN INFERENCE
Wangyang Zhang, **Xin Li** - *Carnegie Mellon Univ., Pittsburgh, PA*
Rob Rutenbar - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

17.2 SPEEDPATH ANALYSIS UNDER PARAMETRIC TIMING MODELS
Luis Guerra e Silva - *INESC-ID/IST - TU Lisbon, Lisboa, Portugal*
Joel R. Phillips - *Cadence Design Systems, Inc., Berkeley, CA*
L. Miguel Silveira - *INESC-ID/IST/Cadence Research Labs - TU Lisbon, Lisboa, Portugal*

17.3 POST-SILICON DIAGNOSIS OF SEGMENTS ON FAILING SPEEDPATHS DUE TO MANUFACTURING VARIATIONS
Lin Xie, **Azadeh Davoodi**, Kewal K. Saluja - *Univ. of Wisconsin, Madison, WI*

18 PLACEMENT: FROM TRADITIONAL TECHNIQUES TO NOVEL CIRCUIT STYLES

Rm: 210CD

Physical Design

Chair: **Bill Halpin** - *Synopsys, Inc., San Jose, CA*

This session contains three interesting papers on placement techniques for emerging layout issues. The first paper presents a multi-level analytical placement algorithm to pulsed-latch-aware placement for timing integrity. The second paper incorporates a history-based scheme into a legalization algorithm using min-cost flow. The third paper proposes an algorithm to handle both boundary and symmetry constraints in analog placement.

18.1 PULSED-LATCH-AWARE PLACEMENT FOR TIMING-INTEGRITY OPTIMIZATION
Yi-Lin Chuang, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Sangmin Kim, Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

18.2 HISTORY-BASED VLSI LEGALIZATION USING NETWORK FLOW
Minsik Cho, Haoxing Ren, Hua Xiang, Ruchir Puri - *IBM Corp., Yorktown Hts., NY*

18.3 PERFORMANCE-DRIVEN ANALOG PLACEMENT CONSIDERING BOUNDARY CONSTRAINT
Cheng-Wu Lin, Jai-Ming Lin, Chun-Po Huang, Soon-Jyh Chang - *National Cheng Kung Univ., Tainan, Taiwan*

TECHNICAL SESSIONS

Wednesday, June 16 9:00 - 11:00am

19 PANEL: 3-D STACKED DIE: NOW OR THE FUTURE?

Rm: 207AB

Physical Design

Chair: **Andrew Yang** - *Apache Design Solutions, Inc., San Jose, CA*
Organizers: **Samta Bansal** - *Cadence Design Systems, Inc., San Jose, CA*
Juan Rey - *Mentor Graphics Corp., San Jose, CA*

The continuation of Moore's law by conventional CMOS scaling is a major upcoming challenge. 3-D Packaging with 3-D through silicon vias (TSV) interconnects shows promise for extending scaling using mature silicon technologies, providing another path towards the 'More than Moore'. Two years ago, the big unceasing question was "Why 3-D?" Today, as we move forward with the concrete implementation of the technology, the questions that are asked, now are "When 3-D?" and "How 3-D?" There are quite a few brave souls who have taken this disruptive interconnect technology and are investing in it today. However, for many lingering questions that remain include "Are we there yet?" and "Is it now or the future?". This panel brings together key thought leaders in the area of 3-D Packaging with 3-D TSV interconnects. how they see 3-D integrated circuits shaping up in the coming year(s) and future challenges associated with TSV in practical design.

Speakers:
Myung-Soo Jang - *Samsung, Yongin-City, Gyeonggi-Do, Republic of Korea*
LC Lu - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*
Philippe Magarshack - *STMicroelectronics, Crolles, France*
Marchal Pol - *IMEC, Leuven, Belgium*
Riko Radojcic - *Qualcomm, Inc., San Diego, CA*

20 SPECIAL SESSION: A DECADE OF NOC RESEARCH - WHERE DO WE STAND?

Rm: 209AB

System-Level and Embedded

Chair: **Grant Martin** - *Tensilica, Inc., Santa Clara, CA*
Organizers: **Sri Parameswaran** - *Univ. of New South Wales, Sydney, Australia*
Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

It is around ten years since Networks-on-Chips (NOCs) emerged as an active research topic. There were widely varying opinions about the prospects for NOCs, ranging from "This is the future of on-chip interconnect" to "It will never work". The session will bring together prominent researchers and practitioners from the domain of on-chip communication architecture to look back at the decade of progress on this topic, and (i) evaluate where NOCs stand in terms of maturity as a research area, (ii) examine where they have succeeded and where they have failed, (iii) identify challenges and issues that remain to be addressed, and (iv) predict how they will be used in the next five years. (Are they ready to replace buses as the mainstay architecture for on-chip interconnect? If not, where will NOCs thrive?. The session will conclude with a panel moderated by Grant Martin where speakers will speculate on the future of NOCs.

20.1 NETWORKS ON CHIPS: FROM RESEARCH TO PRODUCTS

Federico Angiolini, Antonio Pullini - *iNoCs, Lausanne, Switzerland*
Luca Benini - *Univ. di Bologna, Bologna, Italy*
Ciprian Seiculescu, **Giovanni De Micheli** - *LSI and Ecole Polytechnique Fédérale de Lausanne, Switzerland*
Srinivasan Murali - *iNoCs, LSI and Ecole Polytechnique Fédérale de Lausanne, Switzerland*

20.2 THE AETHEREAL NETWORK-ON-CHIP AFTER TEN YEARS: GOALS, EVOLUTION, LESSONS, AND FUTURE

Kees Goossens - *Technische Univ. Eindhoven, Eindhoven, The Netherlands*
Andreas Hansson - *Univ. of Twente, Enschede, The Netherlands*

20.3 THE EVOLUTION OF SOC INTERCONNECT AND HOW NOC FITS WITHIN IT

Bruce Mathewson - *ARM Ltd., Cambridge, United Kingdom*

20.4 PANEL ON THE FUTURE OF NOCs

Giovanni De Micheli - *LSI and Ecole Polytechnique Fédérale de Lausanne, Switzerland*
Kees Goossens - *Technische Univ. Eindhoven, Eindhoven, The Netherlands*
Bruce Mathewson - *ARM Ltd., Cambridge, United Kingdom*

21 EXPLOITING CONCURRENCY FOR SYSTEM-LEVEL PERFORMANCE

Rm: 207D

System-Level and Embedded

Chair: **Sungjoo Yoo** - *Pohang Univ. of Science and Technology, Pohang, Republic of Korea*

In this session, multicore, pipelined and multithreaded architectures are used to improve system performance. The first paper proposes a technique to synthesize a multithreaded architecture starting from a data-path specification. The second paper provides analytical results for the performance of a stream of jobs through a pipeline with stochastic performance. The third paper solves the problem of allocating tasks to processors in MPSOCs to guarantee performance under process variation. The last paper provides a worst-case completion time analysis for a set of tasks in a multiprocessor system with shared resources for different access policies.

21.1 AUTOMATIC MULTITHREADED PIPELINE SYNTHESIS FROM TRANSACTIONAL DATA-PATH SPECIFICATIONS

Eriko Nurvitadhi, James C. Hoe - *Carnegie Mellon Univ., Pittsburgh, PA*
Timothy Kam, Shih-Lien L. Lu - *Intel Corp., Hillsboro, OR*

21.2 ON THE COSTS AND BENEFITS OF STOCHASTICITY IN STREAM PROCESSING

Raj Rao Nadakuditi, Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*

21.3 PERFORMANCE YIELD-DRIVEN TASK ALLOCATION AND SCHEDULING FOR MPSOCs UNDER PROCESS VARIATION

Lin Huang, Qiang Xu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

21.4 WORST CASE RESPONSE TIME ANALYSIS OF RESOURCE ACCESS MODELS IN MULTICORE SYSTEMS

Andreas Schranzhofer, Jian-Jia Chen - *ETH Zürich, Switzerland*
Rodolfo Pellizzoni, Marco Caccamo - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Lothar Thiele - *ETH Zürich, Switzerland*

TECHNICAL SESSIONS

Wednesday, June 16 9:00 - 11:00am

22 DATA ACCESS TIMES DEFINE PERFORMANCE!

Rm: 207C

System-Level and Embedded

Chair: **Dirk Stroobandt** - *Ghent Univ., Ghent, Belgium*

This session presents new developments for solving problems in memory organization, simulation, and optimization. The first two papers propose new cache optimizations. The first one presents new hardware to cache IP addresses in high-performance IP routers more efficiently. The second paper proposes an ultra-fast optimization heuristic for locking instruction caches of embedded systems. In the third paper, the problem of reducing the write activities in non-volatile memories is addressed to extend their lifetime. The final paper presents cleverly engineered data structures that exploit newly-discovered properties of round-robin cache replacement policies to speed up the simulation of such caches.

⏩22.1 A NEW IP LOOKUP CACHE FOR HIGH PERFORMANCE IP ROUTERS
Guangdeng Liao, Heeyeol Yu, Laxmi Bhuyan - *Univ. of California, Riverside, CA*

22.2 INSTRUCTION CACHE-LOCKING USING TEMPORAL REUSE PROFILE
Yun Liang, Tulika Mitra - *National Univ. of Singapore, Singapore*

22.3 REDUCING WRITE ACTIVITIES ON NON-VOLATILE MEMORIES IN EMBEDDED CMPS VIA DATA MIGRATION AND RECOMPUTATION
Jingtong Hu, Wei-Che Tseng, Yi He, Edwin H.-M. Sha - *Univ. of Texas, Dallas, Richardson, TX*
Chun Jason Xue - *City Univ. of Hong Kong, Kowloon, Hong Kong*
Meikang Qiu - *Univ. of Kentucky, Lexington, KY*

22.4 SCUD: A FAST SINGLE-PASS L1 CACHE SIMULATION APPROACH FOR EMBEDDED PROCESSORS WITH ROUND-ROBIN REPLACEMENT POLICY
Mohammad Shihabul Haque, Jorgen Peddersen, Andhi Janapsatya, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

23 TOOLS FOR EFFECTIVE POST-SILICON VALIDATION AND TEST

Rm: 210AB

Verification and Test

Chair: **Mehdi Tahoori** - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

Come to this session to learn about exciting advances in validation and test of complex ICs. The first paper shows a test compression technique to reduce the escalating production test costs without sacrificing test quality. The second paper presents new approaches for efficient post-silicon bug localization with results on an industrial microprocessor design. The next paper utilizes learning techniques to explain design versus silicon mismatches. The final paper leverages the parallelism offered by many-core processors to speed up fault simulation essential for debug and diagnostics.

23.1 FULLY X-TOLERANT, VERY HIGH SCAN COMPRESSION
Peter Wohl - *Synopsys, Inc., Williston, VT*
John Waicukauski - *Synopsys, Inc., Tualatin, OR*
Frederic Neuveux - *Synopsys, Inc., Montbonnot, France*
Emil Gizdarski - *Synopsys, Inc., Mountain View, CA*

⏩23.2 BLOG: POST-SILICON BUG LOCALIZATION IN PROCESSORS USING BUG LOCALIZATION GRAPHS
Sung-Boem Park, Subhasish Mitra - *Stanford Univ., Stanford, CA*
Anne C. Bracy - *Washington Univ. and Microarchitecture Research Lab, Intel Labs, St. Louis, MO*
Hong Wang - *Intel Corp., Santa Clara, CA*

⏩23.3 CLASSIFICATION RULE LEARNING USING SUBGROUP DISCOVERY OF CROSS-DOMAIN ATTRIBUTES RESPONSIBLE FOR DESIGN-SILICON MISMATCH
Nicholas Callegari, Dragoljub (Gagi) Drmanac, Li-C. Wang - *Univ. of California, Santa Barbara, CA*
Magdy S. Abadir - *Freescale Semiconductor, Inc., Austin, TX*

23.4 EFFICIENT FAULT SIMULATION ON MANY-CORE PROCESSORS
Michael A. Kochte, Marcel Schaal, Hans-Joachim Wunderlich, Christian G. Zoellin - *Univ. of Stuttgart, Stuttgart, Germany*

24 SHAPES AND STATISTICS: MANUFACTURABILITY AND YIELD

Rm: 210CD

DFM and the Manufacturing Interface

Chair: **Puneet Sharma** - *Freescale Semiconductor, Inc., Austin, TX*

This session spans use of statistics in circuit analysis to combinatorics in lithographic analysis. The first paper gives methods to extract representative critical paths and path segments for post-silicon prediction. The second paper presents a very fast approach for circuit-level yield analysis. The third paper presents a simple but interesting frequency domain approach for layout decomposition in double-dipole lithography. The fourth paper extends a gridless detailed router to account for double patterning conflicts. The final paper electrically models and optimizes contact shapes in presence of lithographic variation.

24.1 REPRESENTATIVE PATH SELECTION FOR POST-SILICON TIMING PREDICTION UNDER VARIABILITY
Lin Xie, **Azadeh Davoodi** - *Univ. of Wisconsin, Madison, WI*

24.2 QUICKYIELD: AN EFFICIENT GLOBAL-SEARCH BASED PARAMETRIC YIELD ESTIMATION WITH PERFORMANCE CONSTRAINTS
Fang Gong, Yiyu Shi, Daesoo Kim, Lei He - *Univ. of California, Los Angeles, CA*
Hao Yu - *Nanyang Technological Univ., Singapore, Singapore*
Junyan Ren - *Fudan Univ., Shanghai, China*

24.3 DOUBLE PATTERNING LITHOGRAPHY AWARE GRIDLESS DETAILED ROUTING WITH INNOVATIVE CONFLICT GRAPH
Yen-Hung Lin, Yih-Lang Li - *National Chiao Tung Univ., Hsinchu, Taiwan*

24.4S FREQUENCY DOMAIN DECOMPOSITION OF LAYOUTS FOR DOUBLE DIPOLE LITHOGRAPHY
Kanak Agarwal - *IBM Corp., Austin, TX*

24.5S COMPACT MODELING AND ROBUST LAYOUT OPTIMIZATION FOR CONTACTS IN DEEP SUB-WAVELENGTH LITHOGRAPHY
Yongchan Ban, David Z. Pan - *Univ. of Texas, Austin, TX*

TECHNICAL SESSIONS

Wednesday, June 16 2:00 - 4:00pm

25 PANEL: DOES IC DESIGN HAVE A FUTURE IN THE CLOUDS?

Rm: 207AB

Business

Chair: **Raul Camposano** - *Consultant, Cupertino, CA*
Organizer: **Andreas Kuehlmann** - *Cadence Design Systems, Inc., Berkeley, CA*

In a nutshell, cloud computing is a bundled service of software running on remote data centers. Customers can 'rent' these hardware and software resources on-demand, avoiding large investments. The current popularity of cloud computing is driven by the cost-effective on-demand availability of large, scalable amounts of computing resources. The cloud has become an established paradigm for many enterprise and consumer applications such as email, web servers, productivity applications, customer relationship management, etc. However, in IC design its success is still limited. This panel will discuss the real and perceived hurdles that currently prevent a broad adoption of cloud computing in IC design including:

- Security: Safeguarding of large amounts design data
- Scaling: Broad availability of not only many, but also very large servers with large amounts of memory, storage and data transfer bandwidth
- Algorithms: Algorithms and flows that scale well for a large number of servers with uncertain latency and increased failure rates
- Business models: EDA leases tools for years while the predominant business model on the cloud is SaaS and pay-as-you-go
- Technical issues: Other issues include error recovery, availability, performance unpredictability, lock in...

Speakers:
John Chilton - *Synopsys, Inc., Mountain View, CA*
Paul Leventis - *Altera Corp., San Jose, CA*
Rean Griffith - *Univ. of California, Berkeley, CA*
James Colgan - *Xuropa, Inc., San Francisco, CA*
Samuel George - *Cadence Design Systems, Inc., Toronto, ON, Canada*
Deepak Singh - *Amazon.com, Inc., Seattle, WA*

26 SPECIAL SESSION: THE ANALOG MODEL CRISIS – HOW CAN WE SOLVE IT?

Rm: 209AB

Analog/Mixed-Signal/RF Design

Chair: **Kevin D. Jones** - *City Univ., London, United Kingdom and Green Plug, Inc., San Ramon, CA*
Organizer: **Jaeha Kim** - *Seoul National Univ., Seoul, Republic of Korea*

The "analog model crisis" is real and plaguing many mixed-signal systems being designed today. There are so many disagreements regarding the best practices with analog models, such as:

- Who should be writing the models - the system architect, the system verifier, or the block-level circuit designer?
- What should be included in the models - just the functional behavior or also the detailed non-idealities?
- How should we verify them - extract correct models by construction or verify them via equivalence checks?
- Unfortunately, the resulting confusion often allows even trivial bugs to escape detection, with no means of identifying their source.

This session aims to quench the thirst for the best practices and tools with analog models – how to get them, how to use them, and how to make sure they are correct. Three prominent researcher--who have strong, but different opinions on this matter--each representing theoreticians, EDA tool developers, and circuit/system designers, will give brief presentations on their views. The session concludes with a panel that will discuss the best ways to solve the current analog model crisis.

26.1 AUTOMATED COMPACT DYNAMICAL MODELING: AN ENABLING TOOL FOR ANALOG DESIGNERS
Bradley Bond, **Luca Daniel** - *Massachusetts Institute of Technology, Cambridge, MA*

26.2 MODEL-BASED FUNCTIONAL VERIFICATION
Henry Chang, **Ken Kundert** - *Designer's Guide Consulting, Inc., Los Altos, CA*

26.3 FORTIFYING ANALOG MODELS WITH EQUIVALENCE CHECKING AND COVERAGE ANALYSIS
Mark A. Horowitz, James Mao, Sabrina Liao, Frances Lau, Byong Chan Lim, Metha Jeeradit - *Stanford Univ., Stanford, CA*

26.4 PANEL SESSION ON THE ANALOG MODEL CRISIS
Luca Daniel - *Massachusetts Institute of Technology, Cambridge, MA*
Ken Kundert - *Designer's Guide Consulting, Inc., Los Altos, CA*
Mark Horowitz - *Stanford Univ., Stanford, CA*

27 APPLICATION-DRIVEN NETWORK-ON-CHIP DESIGN

Rm: 207D

System-Level and Embedded

Chair: **Jörg Henkel** - *Univ. Karlsruhe, Karlsruhe, Germany*

Networks-On-Chip have been proposed as an approach to design interconnects for future ICs. This session explores the importance of customizing the NOC design to suit application characteristics. The first paper proposes a methodology to use emulation to evaluate NOC designs for many-core processors. The second and third papers propose application-driven approaches to virtual channel allocation and routing. The fourth paper proposes hardware that can be used to predict future traffic patterns based on the past, similar to branch prediction in microprocessors. The last paper discusses how the NOC can be optimized for more efficient off-chip memory access.

27.1 AUTOMATED MODELING AND EMULATION OF INTERCONNECT DESIGNS FOR MANY-CORE CHIP MULTIPROCESSORS
Colin J. Ihrig, Rami G. Melhem, Alex K. Jones - *Univ. of Pittsburgh, Pittsburgh, PA*

27.2 TRACE-DRIVEN OPTIMIZATION OF NETWORKS-ON-CHIP CONFIGURATIONS
Andrew B. Kahng, Bill Lin, **Kambiz Samadi**, Rohit Sunkam Ramanujam - *Univ. of California at San Diego, La Jolla, CA*

27.3 ACES: APPLICATION-SPECIFIC CYCLE ELIMINATION AND SPLITTING FOR DEADLOCK-FREE ROUTING ON IRREGULAR NETWORK-ON-CHIP
Jason Cong, **Chunyue Liu**, Glenn Reinman - *Univ. of California, Los Angeles, CA*

27.4S NTPT: ON THE END-TO-END TRAFFIC PREDICTION IN THE ON-CHIP NETWORKS
Yoshi Shih-Chieh Huang, Kaven Chun-Kai Chou, Chung-Ta King - *National Tsing-Hua Univ., Hsinchu, Taiwan*
Shau-Yin Tseng - *Industrial Technology Research Institute, Hsinchu, Taiwan*

27.5S APPLICATION-AWARE NOC DESIGN FOR EFFICIENT SDRAM ACCESS
Wooyoung Jang, David Z. Pan - *Univ. of Texas, Austin, TX*

TECHNICAL SESSIONS

Wednesday, June 16 2:00 - 4:00pm

28 EXPLOITING FPGA-SPECIFIC FEATURES FOR ROBUSTNESS AND EFFICIENCY

Rm: 207C

Synthesis and FPGA

Chair: **Sudip Nag** - *Xilinx, Inc., San Jose, CA*

This session focuses on the differences between FPGAs and ASICs and how tools and applications can exploit those differences. The first paper deals with the rarely addressed problem of mapping user-memories to a set of FPGA memory components. The second paper shows how to create an accurate microarchitectural simulator of a 64-core SPARC processor on a single FPGA. Finally, the third paper shows how a rewiring technique can leverage unused pins and logic to increase the mean time to failure by 25%.

28.1 EMBEDDED MEMORY BINDING IN FPGAs
Kaveh G. Elizeh, Nicola Nicolici - *McMaster Univ., Hamilton, ON, Canada*

28.2 RAMP GOLD: AN FPGA-BASED ARCHITECTURE SIMULATOR FOR MULTIPROCESSORS
Zhangxi Tan, Andrew Waterman, Rimas Avizienis, Yunsup Lee, Henry Cook, David Patterson, Krste Asanovic - *Univ. of California, Berkeley, CA*

⏩28.3 REWIRING FOR ROBUSTNESS
Manu Jose - *Univ. of California, Los Angeles, CA*
Yu Hu - *Univ. of Alberta, Edmonton, AB, Canada*
Lei He, Rupak Majumdar - *Univ. of California, Los Angeles, CA*

29 LEAKAGE ESTIMATION AND OPTIMIZATION

Rm: 210AB

Low-Power Design

Chair: **Wenjie Jiang** - *Intel Corp., Santa Clara, CA*

As leakage becomes a significant part of total power budgets, leakage estimation and leakage-aware design techniques at all levels of the design hierarchy become increasingly important. This session includes algorithms for full-chip leakage estimation based on statistical treatment of on-die variations. Also included is a synthesis approach for fine-grained power gating for active mode leakage reduction at the gate-level. The final paper deals with leakage at a higher level and presents a leakage-aware run-time adaptive scheduling algorithm for multiprocessor systems.

29.1 EFFICIENT TAIL ESTIMATION FOR MASSIVE CORRELATED LOG-NORMAL SUMS - WITH APPLICATIONS IN STATISTICAL LEAKAGE ANALYSIS
Mingzhi Gao, Zuochang Ye, Yan Wang, Zhiping Yu - *Tsinghua Univ., Beijing, China*

29.2 A LINEAR ALGORITHM FOR FULL-CHIP STATISTICAL LEAKAGE POWER ANALYSIS CONSIDERING WEAK SPATIAL CORRELATION
Ruijing Shen, Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*
Jinjun Xiong - *IBM Corp., Yorktown Hts., NY*

29.3 SYNTHESIS AND IMPLEMENTATION OF ACTIVE MODE POWER GATING CIRCUITS
Jun Seomun, Insup Shin, Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

29.4 LEAKAGE-AWARE DYNAMIC SCHEDULING FOR REAL-TIME ADAPTIVE APPLICATIONS ON MULTIPROCESSOR SYSTEMS
Heng Yu, Bharadwaj Veeravalli, Yajun Ha - *National Univ. of Singapore, Singapore*

30 LOGIC SYNTHESIS IS ALIVE AND KICKING

Rm: 210CD

Synthesis and FPGA

Chair: **Philip Brisk** - *Univ. of California, Riverside, CA*

This session presents four novel contributions in the area of logic synthesis. The first paper described a new SAT-based algorithm for NPN matching of Boolean functions, which complements other techniques and generalizes to incompletely specified function. The second paper presents a fast ATPG-based method for circuit compression, which adds and removes nodes in the presence of don't-cares. The third paper extends the use of ATPG-based redundancy addition and removal to increase fault tolerance of logic. The last, but not the least, is the paper which proposes to use Boolean methods for increasing fault tolerance of FPGA designs by modifying technology mapping to select LUTs containing fewer care bits.

⏩30.1 BooM: A DECISION PROCEDURE FOR BOOLEAN MATCHING WITH ABSTRACTION AND DYNAMIC LEARNING
Chih-Fan Lai, **J.-H. Roland Jiang** - *National Taiwan Univ., Taipei, Taiwan*
Kuo-Hua Wang - *Fu Jen Catholic Univ., Taipei, Taiwan*

⏩30.2 NODE ADDITION AND REMOVAL IN THE PRESENCE OF DON'T CARES
Yung-Chih Chen, Chun-Yao Wang - *National Tsing-Hua Univ., Hsinchu, Taiwan*

30.3 ECR: A LOW COMPLEXITY GENERALIZED ERROR CANCELLATION REWIRING SCHEME
Xiaoqing Yang, Tak Kei Lam, Yu-Liang Wu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

30.4 LUT-BASED FPGA TECHNOLOGY MAPPING FOR RELIABILITY
Jason Cong, **Kirill Minkovich** - *Univ. of California, Los Angeles, CA*

TECHNICAL SESSIONS

Wednesday, June 16 4:30 - 6:00pm

31 PANEL: WHAT'S COOL FOR THE FUTURE OF ULTRA-LOW-POWER DESIGNS?

Rm: 207AB

Low-Power Design

Chair: **John Blyler** - *Chip Design Magazine, San Francisco, CA*
Organizer: **Nagaraj NS** - *Texas Instruments, Inc., Dallas, TX*

Ultra-low-power and energy efficiency requirements are common to most IC designs today. Requirements range from extending battery life to operating on harvested energy, with applications ranging from consumer electronics to medical applications. Design methodologies have evolved over the past decade to cater to low-power designs. This panel will discuss the design methodology challenges in the next generation ultra-low-power and energy efficient IC designs, covering EDA roadmapping, low-power standards, and design and verification flows.

Speakers:
S Balajee - *Texas Instruments, Inc., Bangalore, India*
Alan Gibbons - *Synopsys, Inc., Reading, United Kingdom*
Koorosh Nazifi - *Cadence Design Systems, Inc., San Jose, CA*
Venugopal Puvvada - *Qualcomm, Inc., Bangalore, India*
Toshiyuki Saito - *Renesas Technology Corp., Kawasaki, Japan*

32 SPECIAL SESSION: DESIGN CLOSURE FOR RELIABILITY

Rm: 209AB

Verification and Test

Chair: **Masahiro Fujita** - *Univ. of Tokyo, Tokyo, Japan*
Organizer: **Görschwin Fey** - *Univ. Bremen, Bremen, Germany*

Shrinking feature sizes are making reliability the hot topic in design – in the near future reliability may be the single most important design goal. Traditional measures like cost, speed, etc. will become subordinate. Reliability has to be considered at every design level from technology at the low end up to the system level. Therefore reliability analysis must become an integral part of the design flow, i.e., design closure for reliability is required. The speakers of the special session will show:

- Advanced techniques to implement reliability
- Powerful methods to verify reliability
- Repair techniques that can be used in field, if nothing else helped

32.1 VERIFICATION FOR FAULT TOLERANCE OF THE IBM SYSTEM Z MICROPROCESSOR

Brian W. Thompto - *IBM Corp., Austin, TX*
Bodo Hoppe - *IBM Corp., Boeblingen, Germany*

32.2 FORMAL MODELING AND REASONING FOR RELIABILITY ANALYSIS

Natasa Miskov-Zivanov - *Univ. of Pittsburgh, Pittsburgh, PA*
Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

32.3 USING INTROSPECTIVE SOFTWARE-BASED TESTING FOR POST-SILICON DEBUG AND REPAIR

Todd M. Austin - Advanced Micro Devices, Inc. - *Univ. of Michigan, Ann Arbor, MI*

33 ENERGY-EFFICIENT EMBEDDED HARDWARE DESIGN AND MANAGEMENT

Rm: 207D

System-Level and Embedded

Chair: **Lars Bauer** - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

This session focuses on the design of energy-efficient embedded hardware. The first paper describes the design of a SIMD processor that supports low-voltage operation. The second paper describes static and dynamic techniques for memory optimization in embedded systems. The third paper describes a technique to use the error resilience of some embedded applications to improve energy efficiency.

⏩33.1 XETAL-PRO: AN ULTRA-LOW ENERGY AND HIGH THROUGHPUT SIMD PROCESSOR

Yifan He, Yu Pu, Zhenyu Ye, Sebastian M. Londono, **Henk Corporaal** - *Technische Univ. Eindhoven, Eindhoven, The Netherlands*
Anteneh A. Abbo - *Philips Semiconductor, Eindhoven, The Netherlands*
Richard Kleihorst - *VITO and Ghent Univ., Ghent, Belgium*

33.2 A FRAMEWORK FOR AUTOMATIC PARALLELIZATION, STATIC AND DYNAMIC MEMORY OPTIMIZATION IN MPSOC PLATFORMS

Yiannis Iosifidis - *National Technical Univ. of Athens, Athens, Greece*
Arindam Mallik, Stylianos Mamagkakis, Eddy De Greef - *IMEC, Leuven, Belgium*
Alexandros Bartzas - *Democritus Univ. of Thrace, Xanthi, Greece*
Dimitrios Soudris - *National Technical Univ. of Athens, Athens, Greece*
Francky Catthoor - *IMEC, Leuven, Belgium*

33.3 SCALABLE EFFORT HARDWARE DESIGN: EXPLOITING ALGORITHMIC RESILIENCE FOR ENERGY EFFICIENCY

Vinay K. Chippa, Debabrata Mohapatra, Anand Raghunathan, Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Srimat T. Chakradhar - *NEC Corp., Princeton, NJ*

TECHNICAL SESSIONS

Wednesday, June 16 4:30 - 6:00pm

34 PARALLEL AND EFFICIENT TECHNIQUES IN CIRCUIT SIMULATION

Rm: 207C

Analog/Mixed-Signal/RF Design

Chair: **Xin Li** - *Carnegie Mellon Univ., Pittsburgh, PA*

This session covers a range of relevant topics in parallel circuit simulation on multicore platforms, RF steady-state simulation, and SRAM dynamic stability analysis. The first paper in the session describes an approach for run-time performance modeling for parallel multi-algorithm circuit simulation. The second paper is on SRAM dynamic stability analysis based on a tangent hyperplane approximation for the seperatrix in a high-dimensional space. The last paper presents an improved algorithm for performing periodic steady-state analysis of RF circuits based on the exploitation of the cyclic-block structure of the Jacobian matrices in an iterative Krylov-subspace based solver.

34.1 PARALLEL PROGRAM PERFORMANCE MODELING FOR RUN-TIME OPTIMIZATION OF MULTI-ALGORITHM CIRCUIT SIMULATION
Xiaoji Ye, Peng Li - *Texas A&M Univ., College Station, TX*

34.2 SEPARATRICES IN HIGH-DIMENSIONAL STATE SPACE: SYSTEM-THEORETICAL TANGENT COMPUTATION AND APPLICATION TO SRAM DYNAMIC STABILITY ANALYSIS
Yong Zhang, Peng Li, Garng M. Huang - *Texas A&M Univ., College Station, TX*

34.3 A ROBUST PERIODIC ARNOLDI SHOOTING ALGORITHM FOR EFFICIENT ANALYSIS OF LARGE-SCALE RF/MMICs
Xue-Xin Liu, Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*
Hao Yu - *Nanyang Technological Univ., Singapore, Singapore*

35 THERMAL MANAGEMENT AND OPTIMIZATION

Rm: 210AB

Low-Power Design

Chair: **Garrett Rose** - *Polytechnic Institute of New York Univ., Brooklyn, NY*

Thermal effects have become a first order concern for modern computer systems. The papers in this session focus on thermal management for multicore systems through task migration, on thermal-aware task scheduling for embedded systems with deterministic workload requirements, and on thermal-aware optimization of systems using advanced thin-film thermoelectric local cooling.

35.1 DISTRIBUTED TASK MIGRATION FOR THERMAL MANAGEMENT IN MANY-CORE SYSTEMS
Yang Ge, Parth Malani, **Qinru Qiu** - *Binghamton Univ., Binghamton, NY*

35.2 THERMAL AWARE TASK SEQUENCING ON EMBEDDED PROCESSORS
Sushu Zhang, Karam S. Chatha - *Arizona State Univ., Tempe, AZ*

35.3 A FRAMEWORK FOR OPTIMIZING THERMO-ELECTRIC ACTIVE COOLING SYSTEMS
Jieyi Long, Seda Ogrenci Memik - *Northwestern Univ., Evanston, IL*

36 CATCH OF THE DAY IN BENCHMARKING AND OPTIMAL SYNTHESIS

Rm: 210CD

Synthesis and FPGA

Chair: **Bryan Yu Hu** - *Univ. of Alberta, Edmonton, AB, Canada*

The papers of this session address various topics related to circuit synthesis, with special attention to benchmarking and optimality. The first paper advocates the construction of synthetic representative benchmarks for gate sizing heuristics for which optimal solutions are known by construction. The second paper introduces a metric to detect tangled logic structures in netlists and thus help routability by relaxing placement. The third paper revisits logic synthesis in a special technological context, and shows that optimality is possible in that case. The last paper prunes aggressively the design space of single constant multipliers to address comprehensively 32-bit constants.

36.1 EYECHARTS: CONSTRUCTIVE BENCHMARKING OF GATE SIZING HEURISTICS
Amarnath Kasibhatla, Puneet Gupta - *Univ. of California, Los Angeles, CA*
Puneet Sharma - *Freescale Semiconductor, Inc., Austin, TX*
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

36.2 DETECTING TANGLED LOGIC STRUCTURES IN VLSI NETLISTS
Tanuj Jindal, Jiang Hu - *Texas A&M Univ., College Station, TX*
Charles J. Alpert, Zhuo Li, Gi-Joon Nam, Charles B. Winn - *IBM Corp., Austin, TX*

36.3S LATTICE-BASED COMPUTATION OF BOOLEAN FUNCTIONS
Mustafa Altun, Marc Riedel - *Univ. of Minnesota, Minneapolis, MN*

36.4S A NOVEL OPTIMAL SINGLE CONSTANT MULTIPLICATION ALGORITHM
Jason Thong, Nicola Nicolici - *McMaster Univ., Hamilton, ON, Canada*

TECHNICAL SESSIONS

Thursday, June 16 9:00 - 11:00am

37 PANEL: DESIGNING THE ALWAYS-CONNECTED CAR OF THE FUTURE

Rm: 207AB

System-Level and Embedded

Chair: **Alberto Sangiovanni-Vincentelli** - *Univ. of California, Berkeley, CA*
Organizers: **Arkadeb Ghosal** - *General Motors, Palo Alto, CA*
Paolo Giusto - *General Motors, Palo Alto, CA*

The automotive industry is introducing novel features, such as seamless vehicle-to-vehicle and vehicle-to-infrastructure connectivity to improve in vehicle driver safety (e.g., forward collision warnings) and comfort (e.g., routing to avoid congestion) while facing stricter government regulations, and shortened time-to-market. As a result, automotive Electronic Control System (ECS) architectures are becoming increasingly complex. To cope with these challenges and opportunities, the entire automotive supply chain is engaged as follows: automotive OEMs are managing complexity by reusing legacy components and enabling new technologies; tier one suppliers are increasingly up-integrating features on the same computing platform; tier two suppliers are providing multicore and other powerful technologies; academic institutions are doing research in new analysis, synthesis and optimization methods; and tool providers are trying to raise the level of abstraction for system modeling, analysis and optimization.

The panel will address the following topics:

- What are the challenges and opportunities in this domain?
- What are the new business models among the stakeholders?
- How should academia support in solving the design problems?
- What are the lessons to be learned from the IC design ecosystem?
- How can EDA companies help?

Speakers:
Joseph D'Ambrosio - *General Motors, Warren, MI*
Markus Kühl - *aquintos GmbH, Karlsruhe, Germany*
Ed Nuckolls - *Freescale Semiconductor, Inc., Austin, TX*
Jim Tung - *MathWorks, Inc., Natick, MA*
Peter van Staa - *Robert Bosch GmbH, Reutlingen, Germany*
Harald Wihelm - *Continental AG, Auburn Hills, MI*

38 SPECIAL SESSION: WACI: WILD AND CRAZY IDEAS

Rm: 209AB

General Interest

Chair: **William Joyner** - *Semiconductor Research Corp., Research Triangle Pk., NC*
Organizer: **Valeria Bertacco** - *Univ. of Michigan, Ann Arbor, MI*

The WACI session is packed with wild and crazy ideas intended to stimulate discussion: WACI papers present promising and thought-provoking new ideas, not necessarily fully developed to the point of full papers. Presentations range from incorporating user experience as a design parameter, verifying social networks, anticipating heat problems through online emulation and influence models, to modeling architectures with differential equations, diversity in power supply, sticky wires and earning trust by keeping circuits busy. We count on you to ask the wild questions that make the WACI experience complete. The WAClest question will be rewarded a prize.

38.1 FIND YOUR FLOW: INCREASING FLOW EXPERIENCE BY DESIGNING "HUMAN" EMBEDDED SYSTEMS
Chen-Ling Chou, Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Anca Miron - *Univ. of Wisconsin, Oshkosh, WI*

38.2 ELECTRONIC DESIGN AUTOMATION FOR SOCIAL NETWORKS
Andrew W. DeOrio, Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

38.3 REAL TIME EMULATIONS: FOUNDATION AND APPLICATIONS
Azalia Mirhoseini, Yousra Alkabani, Farinaz Koushanfar - *Rice Univ., Houston, TX*

38.4 NETWORK-ON-CHIP DESIGN AND OPTIMIZATION USING SPECIALIZED INFLUENCE MODELS
Cristinel Ababei - *North Dakota State Univ., Fargo, ND*

38.5 CIRCUIT MODELING FOR PRACTICAL MANY-CORE ARCHITECTURE DESIGN EXPLORATION
Dean N. Truong, Bevan M. Baas - *Univ. of California, Davis, CA*

38.6 HIERARCHICAL HYBRID POWER SUPPLY NETWORKS
Farinaz Koushanfar - *Rice Univ., Houston, TX*

38.7 DETACHABLE NANO-CARBON CHIP WITH ULTRA-LOW-POWER
Shinobu Fujita, Shin'ichi Yasuda - *Toshiba Corp., Kawasaki, Japan*
Xiangyu Chen, Deji Akinwande, Dae Sung Lee, Philip H.-S. Wong - *Stanford Univ., Stanford, CA*

38.8 SYNTHESIS OF TRUSTABLE ICS USING UNTRUSTED CAD TOOLS
Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

39 ALGORITHMS AND ARCHITECTURES FOR EMERGING TECHNOLOGIES

Rm: 207D

General Interest

Chair: **Smita Krishnaswamy** - *IBM Corp., Yorktown Hts., NY*

Progress in emerging technologies covered in this session includes microfluidic biochips, quantum circuits and optical interconnect. Given recent laboratory demonstrations, designers are interested in algorithms and tools for resource optimization. To this end, the first two papers schedule operations of microfluidic biochips so as to avoid droplet cross-contamination. Two papers on quantum circuits offer efficient peephole optimizers to reduce qubits and gate counts, respectively, required to perform a given reversible computation. The last paper of the session studies crosstalk noise in optical interconnect and its impact on the design of on-chip networks.

39.1 SYNCHRONIZATION OF WASHING OPERATIONS WITH DROPLET ROUTING FOR CROSS-CONTAMINATION AVOIDANCE IN DIGITAL MICROFLUIDIC BIOCHIPS
Yang Zhao, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

39.2 CROSS-CONTAMINATION AWARE DESIGN METHODOLOGY FOR PIN-CONSTRAINED DIGITAL MICROFLUIDIC BIOCHIPS
Cliff Chiung-Yu Lin - *National Taiwan Univ. and Stanford Univ., Stanford, CA*
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

39.3 REDUCING THE NUMBER OF LINES IN REVERSIBLE CIRCUITS
Robert Wille, Mathias Soeken, Rolf Drechsler - *Univ. Bremen, Bremen, Germany*

39.4S SYNTHESIS OF THE OPTIMAL 4-BIT REVERSIBLE CIRCUITS
Oleg Golubitsky - *Google, Waterloo, ON, Canada*
Sean Falconer - *Stanford Univ., Stanford, CA*
Dmitri Maslov - *Univ. of Waterloo, Waterloo, ON, Canada*

39.5S CROSSTALK NOISE AND BIT ERROR RATE ANALYSIS FOR OPTICAL NETWORK-ON-CHIP
Yiyuan Xie, Mahdi Nikdast, **Jiang Xu,** Qi Li, Xiaowen Wu, Yaoyao Ye, Xuan Wang, Weichen Liu - *Hong Kong Univ. of Science and Technology, Kowloon, Hong Kong*
Wei Zhang - *Nanyang Technological Univ., Singapore, Singapore*

TECHNICAL SESSIONS

Thursday, June 17 9:00 - 11:00am

40 SIMULATION AND MODELING TECHNIQUES FOR DEVICES AND INTERCONNECT

Rm: 207C

Analog/Mixed-Signal/RF Design

Chair: **Luis Miguel Silveira** - *INESC-ID/IST/Cadence Research Labs - TU Lisbon, Lisbon, Portugal*

The first paper adapts numerical techniques for large on-chip power grid analysis to GPU implementation with impressive speedups. The second paper describes a variation-aware parasitic extraction algorithm, whose complexity is almost independent of the number of variation parameters. The third paper provides a method to model transistors subject to layout dependent process-induced stress. Finally, the last two papers explore extensions of fitting-based modeling techniques: the first towards parameterization, the second for improved accuracy.

40.1 PARALLEL MULTIGRID PRE-CONDITIONING ON GRAPHICS PROCESSING UNITS (GPUs) FOR ROBUST POWER GRID ANALYSIS
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*
Zhiyu Zeng - *Texas A&M Univ., Collge Station, TX*

40.2 STOCHASTIC DOMINANT SINGULAR VECTORS METHOD FOR VARIATION-AWARE EXTRACTION
Tarek A. El-Moselhy, Luca Daniel - *Massachusetts Institute of Technology, Cambridge, MA*

40.3 CLOSED-FORM MODELING OF LAYOUT-DEPENDENT MECHANICAL STRESS
Vivek Joshi, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Valeriy Sukharev - *Mentor Graphics Corp., San Jose, CA*
Juan Andres Torres - *Mentor Graphics Corp., Wilsonville, OR*
Kanak Agarwal - *IBM Corp., Austin, TX*

40.4S GENERATING PARAMETRIC MODELS FROM TABULATED DATA
Sanda Lefteriu - *Rice Univ., Houston, TX*
Jan Mohring - *Fraunhofer ITWM, Kaiserslautern, Germany*

40.5S MFTI: MATRIX-FORMAT TANGENTIAL INTERPOLATION FOR MODELING MULTI-PORT SYSTEMS
Yuanzhe Wang, Chi-Un Lei, Grantham K.H. Pang, Ngai Wong - *The Univ. of Hong Kong, Hong Kong*

41 DESIGN OF ULTRA-LOW-POWER SYSTEMS

Rm: 210AB

Low-Power Design

Chair: **Chandramouli Kashyap** - *Intel Corp., Hillsboro, OR*

With green technologies becoming the talk of the town, ultra-low-power design is an area of very active research. This session focuses on the design of ultra-low-power systems addressing a crucial sector in power efficiency. The first paper addresses a universal state of charge algorithm for battery efficiency. The second paper in the session gives a complete design flow for the generation of ultra-low-power wireless sensor architectures. The third paper addresses a new SRAM design technique for ultra low stand-by power and the final paper addresses a novel technique for pre-emptive dynamic voltage scaling for real-time systems using approximation scheme.

41.1 A UNIVERSAL STATE-OF-CHARGE ALGORITHM FOR BATTERIES
Bingjun Xiao, Yiyu Shi, **Lei He** - *Univ. of California, Los Angeles, CA*

41.2 A COMPLETE DESIGN-FLOW FOR THE GENERATION OF ULTRA-LOW-POWER WSN NODE ARCHITECTURES BASED ON MICRO-TASKING
Muhammad Adeel Pasha, Steven Derrien, Olivier Sentieys - *Univ. de Rennes 1, Rennes, France*

41.3 STACKING SRAM BANKS FOR ULTRA-LOW-POWER STAND-BY MODE OPERATION
Adam C. Cabe, Zhenyu Qi, Mircea R. Stan - *Univ. of Virginia, Charlottesville, VA*

41.4 PREDVS: PRE-EMPTIVE DYNAMIC VOLTAGE SCALING FOR REAL-TIME SYSTEMS USING APPROXIMATION SCHEME
Weixun Wang, Prabhat Mishra - *Univ. of Florida, Gainesville, FL*

42 VARIATION-AWARE METHODS FOR SRAMs AND CLOCKS

Rm: 210CD

Physical Design

Chair: **Payam Heydari** - *Univ. of California, Irvine, CA*

In this session novel variation-aware methods for SRAMs and clocks are discussed. The first paper proposes a non-invasive method to measure threshold variations in SRAMs. The second paper discusses a method for doing statistical analysis during the design phase of SRAMs for the purpose of improving the parametric yield. The third paper proposes a mechanism for creating clock to enable pre-bond testability of dies in 3-D stacked ICs. The last paper proposes a method for clock-tree design to support on-chip skew detection and correction.

42.1 IN-SITU CHARACTERIZATION AND EXTRACTION OF SRAM VARIABILITY
Srivatsan Chellappa, **Jia Ni**, Jyothi Velamala, Xiaoyin Yao, Nathan Hindman, Yu (Kevin) Cao, Lawrence Clark, Min Chen - *Arizona State Univ., Tempe, AZ*

42.2 A HOLISTIC APPROACH FOR STATISTICAL SRAM ANALYSIS
Paul Zuber, Petr Dobrovolny, Miguel Miranda - *IMEC, Leuven, Belgium*

42.3 CLOCK-TREE SYNTHESIS WITH PRE-BOND TESTABILITY FOR 3-D STACKED IC DESIGNS
Tak-Yung Kim, Taewhan Kim - *Seoul National Univ., Seoul, Republic of Korea*

42.4 AN EFFICIENT PHASE DETECTOR CONNECTION STRUCTURE FOR THE SKEW SYNCHRONIZATION SYSTEM
Yu-Chien Kao, Hsuan-Ming Chou, Kun-Ting Tsai, Shih-Chieh Chang - *National Tsing-Hua Univ., Hsinchu, Taiwan*

TECHNICAL SESSIONS

Thursday, June 17

Session 43: 2:30 - 4:00pm, **Sessions 44, 45:** 2:00 - 4:00pm

43 PANEL: JOINT USER TRACK PANEL (SESSION 11U) - WHAT WILL MAKE YOUR NEXT DESIGN EXPERIENCE A MUCH BETTER ONE?

Rm: 208AB

General Interest

Organizer: **Thomas Harms** - *Infineon Technologies AG, Munich, Germany*

Top-designers and design engineering managers will present top wish lists for making their next (or even current) design a much better design experience. They will not focus on pie-in-the-sky research topics, but instead describe down to earth challenges designers face in getting their designs out the door. The panelists will use their data and experiences to substantiate their wish lists and address the main question: What needs to change in the design flows and design tools to improve Time-to-Market (TTM) and design quality?

Speakers:
Reynold D'Sa - *Intel Corp., Santa Clara, CA*
Ruud Haring - *IBM Corp., Yorktown Hts., NY*
Derek Urbaniak - *Oracle, Austin, TX*
Guntram Wolski - *Cisco Systems, Inc., San Jose, CA*
James You - *Broadcom Corp., Irvine, CA*

44 SPECIAL SESSION: CYBER-PHYSICAL SYSTEMS DEMYSTIFIED

Rm: 209AB

General Interest

Chair: **Helen Gill** - *National Science Foundation, Arlington, VA*
Organizer: **Rajesh K. Gupta** - *Univ. of California at San Diego, La Jolla, CA*

Cyber-physical systems (CPS) are deeply coupled systems spanning computing (cyber) and physical processes. CPS is a vibrant and emerging area of research that addresses many new research topics that traditionally are not addressed in the cyber or the physical domains. This session demystifies incorrect perceptions about the lack of fundamental challenges by introducing the DAC audience to the important developments in this emerging area. The session features an embedded tutorial on CPS challenges and opportunities, an embedded tutorial on foundational issues in CPS, and two example CPS systems: on healthcare and energy-efficient smart buildings.

44.1 CYBER-PHYSICAL SYSTEMS: THE NEXT COMPUTING REVOLUTION

Ragunathan (Raj) Rajkumar - *Carnegie Mellon Univ., Pittsburgh, PA*
Insup Lee - *Univ. of Pennsylvania, Philadelphia, PA*
Lui Sha - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
John Stankovic - *Univ. of Virginia, Charlottesville, VA*

44.2 CPS FOUNDATIONS

Edward A. Lee - *Univ. of California, Berkeley, CA*

44.3 MEDICAL CYBER-PHYSICAL SYSTEMS

Insup Lee, Oleg Sokolsky - *Univ. of Pennsylvania, Philadelphia, PA*

44.4 CYBER-PHYSICAL ENERGY SYSTEMS: FOCUS ON SMART BUILDINGS

Jan Kleissl, Yuvraj Agarwal - *Univ. of California at San Diego, La Jolla, CA*

45 APPLICATION AND IMPROVEMENT OF DYNAMIC VERIFICATION

Rm: 207D

Verification and Test

Chair: **Dominik Stoffel** - *Technische Univ. Kaiserslautern, Germany*

This session discusses improvements of dynamic verification techniques as well as their applications. The first paper introduces a trace mining based method to localize bugs. The second paper proposes an efficient parallel simulation technique on GPUs. The third paper introduces a test vector generation method for linear analog/mixed-signal circuits. The fourth paper discusses the verification of low-power architectural intent expressed in UPF. The last paper proposes a technique to speed up simulation when oscillating loops are dynamically detected.

45.1 SCALABLE SPECIFICATION MINING FOR VERIFICATION AND DIAGNOSIS

Wenchao Li, Sanjit A. Seshia - *Univ. of California, Berkeley, CA*
Alessandro Forin - *Microsoft Corp., Redmond, WA*

45.2 DISTRIBUTED TIME, CONSERVATIVE PARALLEL LOGIC SIMULATION ON GPUs

Bo Wang, Yangdong Deng - *Tsinghua Univ., Beijing, China*
Yuhao Zhu - *Beihang Univ., Beijing, China*

45.3 AN EFFICIENT TEST VECTOR GENERATION FOR CHECKING ANALOG/MIXED-SIGNAL FUNCTIONAL MODELS

Byong Chan Lim, Mark A. Horowitz - *Stanford Univ., Stanford, CA*
Jaeha Kim - *Seoul National Univ., Seoul, Republic of Korea*

45.4S LEVERAGING UPF-EXTRACTED ASSERTIONS FOR MODELING AND FORMAL VERIFICATION OF ARCHITECTURAL POWER INTENT

Aritra Hazra, Srobona Mitra, Pallab Dasgupta, Ajit Pal - *Indian Institute of Technology, Kharagpur, India*
Debabrata Bagchi, Kaustav Guha - *Synopsys, Inc., Bangalore, India*

45.5S EFFICIENT SIMULATION OF OSCILLATORY COMBINATIONAL LOOPS

Morteza Fayyazi, Laurent Kirsch - *Mentor Graphics Corp., Waltham, MA*

TECHNICAL SESSIONS

Thursday, June 16 2:00 - 4:00pm

46 TIMING ANALYSIS AND CIRCUIT OPTIMIZATION FOR NOVEL TECHNOLOGIES AND DFM

Rm: 207C

Verification and Test

Chair: **Michael Orshansky** - *Univ. of Texas, Austin, TX*

This session deals with static timing analysis and circuit optimization for novel circuit technologies and design for manufacturability. The first paper describes a novel technique of variation-aware transistor sizing for circuit yield optimization. The second paper presents application of stochastic differential equations to variation-aware circuit simulation. The proposed technique can be used both for transistor level statistical timing and statistical library characterization. The third paper discusses highly parallel implementation of Monte-Carlo analysis on Graphics Processing Units. The last two short papers present static timing of flexible thin-film transistor integrated circuits and 3-D integrated circuits with through-silicon vias.

46.1 TRANSISTOR SIZING OF CUSTOM HIGH-PERFORMANCE DIGITAL CIRCUITS WITH PARAMETRIC YIELD CONSIDERATIONS

Daniel K. Beece, Jinjun Xiong, Vladimir Zolotov - *IBM Corp., Yorktown Hts., NY*
Chandu Visweswariah - *IBM Corp., Hopewell Jct., NY*
Yifang Liu - *Texas A&M Univ., College Station, TX*

46.2 RDE-BASED TRANSISTOR-LEVEL GATE SIMULATION FOR STATISTICAL STATIC TIMING ANALYSIS

Qin Tang, Amir Zjajo, **Michel Berkelaar**, Nick van der Meijs - *Delft Univ. of Technology, The Netherlands*

46.3 EFFICIENT SMART MONTE CARLO-BASED SSTA ON GRAPHICS PROCESSING UNITS WITH IMPROVED RESOURCE UTILIZATION

Vineeth Veetil, Yung-Hsu Chang, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

46.4S STATIC TIMING ANALYSIS FOR FLEXIBLE TFT CIRCUITS

Chao-Hsuan Hsu, **Chester M. Liu**, En-Hua Ma, James Chien-Mo Li - *National Taiwan Univ., Taipei City, Taiwan*

46.5S TSV STRESS-AWARE TIMING ANALYSIS WITH APPLICATIONS TO 3-D-IC LAYOUT OPTIMIZATION

Jae-Seok Yang, David Z. Pan - *Univ. of Texas, Austin, TX*
Krit Athikulwongse, Young-Joon Lee, Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

47 SYSTEM POWER MODELING AND MANAGEMENT

Rm: 210AB

Low-Power Design

Chair: **Yuan Xie** - *Pennsylvania State Univ., State College, PA*

As technology node scales down, system-level power modeling and management become very critical to optimize the power and reliability of large scale computing systems, such as multicore CPUs and embedded SOCs. In this session, four new works address this important task. The first paper presents a Gaussian mixture model to predict the dynamic power usage of virtualized machines. The second paper develops a multiprogrammed, multicore model for estimating performance and power consumption under various workloads. The third paper studies power management for real-time embedded systems under reliability constraint, and the final paper discusses a new design methodology to minimize power when error-tolerance is considered in the processor design.

47.1 A SYSTEM FOR ONLINE POWER PREDICTION IN VIRTUALIZED ENVIRONMENTS USING GAUSSIAN MIXTURE MODELS

Gaurav Dhiman, Kresimir Mihic, Tajana Simunic Rosing - *Univ. of California at San Diego, La Jolla, CA*

47.2 PERFORMANCE AND POWER MODELING IN A MULTI-PROGRAMMED MULTICORE ENVIRONMENT

Xi Chen, Robert P. Dick, Zhuoqing Morley Mao - *Univ. of Michigan, Ann Arbor, MI*
Chi Xu - *Univ. of Minnesota, Minneapolis, MN*

47.3 RELIABILITY AWARE POWER MANAGEMENT FOR DUAL-PROCESSOR REAL-TIME EMBEDDED SYSTEMS

Ranjani Sridharan, Rabi Mahapatra - *Texas A&M Univ., College Station, TX*

47.4 RECOVERY-DRIVEN DESIGN: A POWER MINIMIZATION METHODOLOGY FOR ERROR-TOLERANT PROCESSOR MODULES

Andrew B. Kahng, **Seokhyeong Kang** - *Univ. of California at San Diego, La Jolla, CA*
Rakesh Kumar, John Sartori - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

48 MANAGEMENT OF POWER INTEGRITY AND CIRCUIT RELIABILITY

Rm: 210CD

Interconnect and Reliability

Chair: **Takashi Sato -** *Kyoto Univ., Kyoto, Japan*

VLSI design with scaled CMOS technology is dramatically challenged by an ever-increasing trend of reliability degradation, especially in power supply and on-chip memory. This session presents five papers to address sensing, diagnosis, and protection of circuit reliability. The first two papers develop analysis techniques for power delivery network, while the third paper presents an algorithm for de-cap budgeting. Using a specially designed SRAM cell, the fourth paper proposes a new aging sensor. Finally, the last paper copes with efficient statistical prediction of SRAM failure rate.

48.1 TRADE-OFF ANALYSIS AND OPTIMIZATION OF POWER DELIVERY NETWORKS WITH ON-CHIP VOLTAGE REGULATION

Zhiyu Zeng, Xiaoji Ye, Peng Li - *Texas A&M Univ., College Station, TX*
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

48.2 AN EFFICIENT DUAL ALGORITHM FOR VECTORLESS POWER GRID VERIFICATION UNDER LINEAR CURRENT CONSTRAINTS

Xuanxing Xiong, Jia Wang - *Illinois Institute of Technology, Chicago, IL*

48.3 PARALLEL HIERARCHICAL CROSS ENTROPY OPTIMIZATION FOR ON-CHIP DECAP BUDGETING

Xueqian Zhao, Yonghe Guo, Zhuo Feng, Shiyan Hu - *Michigan Technological Univ., Houghton, MI*

48.4S SRAM-BASED NBTI/PBTI SENSOR SYSTEM DESIGN

Zhenyu Qi, Jiajing Wang, Adam C. Cabe, Stuart Wooters, Travis N. Blalock, Benton H. Calhoun, Mircea R. Stan - *Univ. of Virginia, Charlottesville, VA*

48.5S A STATISTICAL SIMULATION METHOD FOR RELIABILITY ANALYSIS OF SRAM CORE-CELLS

Renan Alves Fonseca, Luigi Dilillo, Alberto Bosio, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel - *LIRMM, Montpellier, France*
Nabil Badereddine - *Infineon Tech., Sophia-Antipolis, France*

TECHNICAL SESSIONS

Thursday, June 16 4:30 - 6:00pm

49 PANEL: WHAT INPUT LANGUAGE IS THE BEST CHOICE FOR HIGH-LEVEL SYNTHESIS (HLS)?

Rm: 207AB

System-Level and Embedded

Chair: **Dan Gajski** - *Univ. of California, Irvine, CA*
Organizers: **Todd Austin** - *Univ. of Michigan, Ann Arbor, MI*
Steve Brown - *Cadence Design Systems, Inc., San Jose, CA*

As of 2010, over 30 of the world's top semiconductor/systems companies have adopted HLS. In 2009, tape-outs for SOCs containing IP developed with HLS exceeded 50 for the first time. Now that the practicality and value of HLS is established, engineers are asking the question of "what input-language works best?" The answer to this question is critical because it drives key decisions regarding the tool/methodology infrastructure companies will create around this new flow. ANSI-C/C++ advocates cite ease-of-learning and simulation speed. SystemC advocates make similar claims, and point to SystemC's hardware-oriented features. Proponents of BSV (Bluespec SystemVerilog) claim that the language enhances architectural transparency and control. To realize the full benefits of HLS, companies must consider all of these factors and then make a choice that is right for their flow..

Speakers:
Vinod Kathail - *Synfora, Inc., Mountain View, CA*
Anmol Mathur - *Calypto Design Systems, Santa Clara, CA*
Michael McNamara - *Cadence Design Systems, Inc., San Jose, CA*
Rishiyur Nikhil - *Bluespec, Inc., Waltham, MA*
John Sanguinetti - *Forte Design Systems, San Jose, CA*
Andres Takach - *Mentor Graphics Corp., Wilsonville, OR*
Devadas Varma - *AutoESL Design Technologies, Inc., San Francisco, CA*

50 SPECIAL SESSION: COMPUTING WITHOUT GUARANTEES

Rm: 209AB

System-Level and Embedded

Chair: **Fadi Kurdahi** - *Univ. of California, Irvine, CA*
Organizer: **Jörg Henkel** - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

The process of electronic system design has traditionally conformed to an axiom – that the specification and implementation need to be equivalent in a numerical or Boolean sense. However, a wide range of application domains, ranging from digital signal processing, multi-media processing, and wireless communications actually do not require such a strong notion of equivalence, due to the presence of noise in the input data and the limited perceptualability of humans consuming their output. Emerging workloads of the future, such as Recognition, Mining, and Synthesis, take this "inherent resilience" to a different level due to the massive amounts of data they process, statistical nature of the algorithms, and built-in expectation of less than perfect results. Several recent research efforts attempt to exploit this inherent resilience of algorithms to obtain unprecedented levels of performance or energy-efficiency in hardware and software implementations.

50.1 STOCHASTIC COMPUTATION

Naresh Shanbhag, Rami Abdallah, Rakesh Kumar, Douglas Jones - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

50.2 BEST-EFFORT AND RE-THINKING

Srimat Chakradhar - *NEC Corp., Princeton, NJ*
Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

50.3 HARDWARE THAT PRODUCES BOUNDED RATHER THAN EXACT RESULTS

Melvin Breuer - *Univ. of Southern California, Los Angeles, CA*

51 DESIGN AND MODELING OF TECHNOLOGIES BEYOND CMOS

Rm: 207D

General Interest

Chair: **Dmitri Strukov** - *Univ. of California, Santa Barbara, CA*

Challenges of extremely scaled silicon motivate the exploration of materials and devices that offer superior characteristics to silicon. This session explores four promising technologies: CNTs, graphene, memristors, and NEMs switches. The first paper models the impact of geometry variation on memristor devices. The second paper explores the design and modeling of a novel graphene gate structure that can be integrated with CMOS circuits. The third paper demonstrates the benefits of device alignment to increase correlation thereby reducing yield loss due to statistical assembly of CNTs. The final paper explores the design and modeling of NEMs logic gates.

51.1 IMPACT OF PROCESS VARIATIONS ON EMERGING MEMRISTOR

Dimin Niu, Cong Xu - *Pennsylvania State Univ., University Park, PA*
Yiran Chen - *Seagate Technology, Eden Prairie, MN*
Yuan Xie - *Pennsylvania State Univ., State College, PA*

51.2 RECONFIGURABLE MULTI-FUNCTION LOGIC BASED ON GRAPHENE P-N JUNCTIONS

Sansiri Tanachutiwat, Ji Ung Lee, **Wei Wang,** Chun Yung Sung - *IBM Corp., Yorktown Hts., NY*

51.3S CARBON NANOTUBE CORRELATION: PROMISING OPPORTUNITY FOR CNFET CIRCUIT YIELD ENHANCEMENT

Jie Zhang, Nishant Patil, Albert Lin, H.-S. Philip Wong, Subhasish Mitra - *Stanford Univ., Stanford, CA*
Shashikanth Bobba, Giovanni De Micheli - *LSI and Ecole Polytechnique, Fédérale de Lausanne Lausanne, Switzerland*

51.4S DESIGN AND ANALYSIS OF COMPACT ULTRA-ENERGY-EFFICIENT LOGIC GATES USING LATERALLY-ACTUATED DOUBLE-ELECTRODE NEM

Hamed Dadgour, Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*
Muhammad M. Hussain - *King Abdullah Univ. of Science and Technology, Thuwal, Saudi Arabia*
Casey Smith - *SEMATECH, Austin, TX*

TECHNICAL SESSIONS

Thursday, June 16 4:30 - 6:00pm

52 YIELD-AWARE OPTIMIZATION AND MODELING FOR ANALOG CIRCUITS

Rm: 207C

Analog/Mixed-Signal/RF Design

Chair: **Trent McConaghy** - *Solido Design Automation, Inc., Saskatoon, SK, Canada*

This session covers recent advances in optimization and modeling for mixed-signal circuits. The first paper proposes a method to efficiently generate variability models by leveraging the similarities in their sparsity patterns across multiple modes and corners. The second paper describes practical ways of centering the nominal design points of analog circuits to achieve maximum yield. The third paper analyzes trade-offs between the circuit performances and its yield, based on a genetic algorithm which incorporates the yield as an objective rather than as a constraint. The last paper aims to achieve uniform coverage of the Pareto surface with sample points.

52.1 TOWARD EFFICIENT LARGE-SCALE PERFORMANCE-MODELING OF INTEGRATED CIRCUITS VIA MULTI-MODE/MULTI-CORNER SPARSE REGRESSION
Wangyang Zhang, Tsung-Hao Chen, Ming-Yuan Ting - *Mentor Graphics Corp., San Jose, CA*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

52.2 BEHAVIOR-LEVEL YIELD ENHANCEMENT APPROACH FOR LARGE-SCALED ANALOG CIRCUITS
Chin-Cheng Kuo, Yen-Lung Chen, Li-Yu Chan, I-Ching Tsai, **Chien-Nan Liu** - *National Central Univ., Jung-Li, Taiwan*

52.3S GENERATION OF YIELD-EMBEDDED PARETO-FRONT FOR SIMULTANEOUS OPTIMIZATION OF YIELD AND PERFORMANCES
Yu Liu, Masato Yoshioka, Katsumi Homma, Toshiyuki Shibuya, Yuzi Kanazawa - *Fujitsu Labs. Ltd., Kawasaki, Japan*

52.4S PARETO SAMPLING: CHOOSING THE RIGHT WEIGHTS BY DERIVATIVE PURSUIT
Amith Singhee - *IBM Corp., Yonkers, NY*
Pamela Castalino - *IBM Corp., Hopewell Junction, NY*

53 REDUCING THE COST OF TEST

Rm: 210AB

Verification and Test

Chair: **Mani Soma** - *Univ. of Washington, Seattle, WA*

Test cost is a major concern for any product, but is especially key in non-digital applications. The first paper in this session describes the challenges in testing 3-D CMOS image sensors and identifies design approaches to improve cost and yield. The second paper gives an improved built-in self-test technique to identify the operating current needed for magnetic RAM. The final paper shows how reconfigurability can be exploited to reduce test cost for the emerging class of all-digital PLLs.

53.1 AN ERROR TOLERANCE SCHEME FOR 3-D CMOS IMAGERS
Hsiu-Ming Chang, Kwang-Ting Cheng - *Univ. of California, Santa Barbara, CA*
Jiun-Lang Huang - *National Taiwan Univ., Taipei, Taiwan*
Cheng-Wen Wu, Ding-Ming Kwai - *Industrial Technology Research Institute and National Tsing-Hua Univ., Hsinchu, Taiwan*

53.2 FAST IDENTIFICATION OF OPERATING CURRENT FOR TOGGLE MRAM BY SPIRAL SEARCH
Sheng-Hung Wang, **Ching-Yi Chen,** Cheng-Wen Wu - *National Tsing-Hua Univ., Hsinchu, Taiwan*

53.3 EXPLOITING RECONFIGURABILITY FOR LOW-COST IN-SITU TEST AND MONITORING OF DIGITAL PLLs
Leyi Yin, Peng Li - *Texas A&M Univ., College Station, TX*

54 SPECIAL SESSION: SMART POWER: FROM YOUR CELL PHONE TO YOUR HOME

Rm: 210CD

Low-Power Design

Chair: **Vivek Tiwari** - *Intel Corp., Santa Clara, CA*
Organizer: **Ruchir Puri** - *IBM Corp., Yorktown Hts., NY*

With the drive towards energy efficiency spanning from the cell phones to the power grid supplying our homes energy, this special session will focus on one of the hottest topics facing the world-wide technical community. Not just in design automation, but beyond design automation: "a holistic view on energy efficiency – from cell phones to our home."

54.1 SMART PHONE POWER
Johnny John, Chris Riddle - *Qualcomm, Inc., San Diego, CA*

54.2 WHAT'S SMART ABOUT THE SMART GRID?
Ian Hiskens - *Univ. of Michigan, Ann Arbor, MI*

54.3 ON-DIE POWER GRIDS - THE MISSING LINK
Eli Chiprout - *Intel Corp., Hillsboro, OR*

USER TRACK HIGHLIGHTS

The DAC User Track brings together IC designers from across the globe. The technical program offers a unique opportunity to pick the latest tips and tricks from the industry expert IC designers. The DAC User Track features over 110 presentations on a wide variety of EDA topics. Designers from Intel, IBM, Samsung, TI, Toshiba, Qualcomm, AMD, Freescale and other leading IC companies will present their experiences on effective design flows, methods and tool usage. There is no other way to improve your 'design IQ' in such a short amount of time.

The list of topics is longer and more diverse than ever before, making the User Track of interest to every designer. Low-power is one of the core topics addressed at the system-level, RTL-level and during the Place and Routing stages of design. Find out how to efficiently design for low-power and build the power delivery network on the chip and through the package. Several designers will address dealing with the significant variability at 32nm and below. You will find interesting presentations on variation-robust design methods with ways to quickly converge on a chip that yields. Timing closure is another theme that is addressed by speakers from a several perspectives, both front-end and back-end. Designers will present on innovative ways to partitioning, budgeting and retime. We also feature presentations on several timing-driven ECO physical optimization methods, and highlight several system-level case studies that use Formal Verification. There are too many topics to cover in this brief summary.

The Design Automation Conference and the User Track brings together thousands of like-minded professionals, making this event an opportunity you cannot miss. The User Track runs for three packed days as a parallel track to the DAC program. Learn from expert designers in person, and find out the truth about design tools. Stroll through the DAC trade show, attend keynotes and cutting-edge technical sessions, or just talk to colleagues from other companies. Whether it's for the full three days or just a single day, DAC has it all. Since DAC 2010 is held right next to Disneyland, this is a great opportunity to bring your family along.

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1 TIMING IS EVERYTHING

Rm:208AB

Tuesday, June 15 10:30am - 12:00pm

Physical Design

Moderator: **Srinivas Nori** - *GLOBALFOUNDRIES, San Jose, CA*

Closing timing is the top priority in most IC design projects. A complex chain of EDA tools helps designers meet the timing objectives. In this session presenters from a variety of major design companies will share their solutions for timing closure. At the system level timing budgets must be distributed carefully between the blocks. At the RTL and logic level gates can be pushed through flipflops. Careful on-chip clock distribution is a key requisite for robust variation tolerant timing closure. At the layout level, crosstalk-induced timing problems can be addressed through various surgical operations. The final paper will present a way to validate the actual path delay.

1U.1S A PRECISE TIMING BUDGETING FLOW FOR SIP CO-DESIGN

Joann Lee, Tsung-Ying Tsai, Shi-Hao Chen, Yi-Feng Chen - *Global Unichip Corp., Hsinchu City, Taiwan*

1U.2S RETIMING TRADE-OFF IN HIGH PERFORMANCE GRAPHIC DESIGNS

Raj Varada, Murali Seshadri, Sharon Martin, Ragadeepika Kshatri - *Intel Corp., Santa Clara, CA*

1U.3S A TOOL FOR EXPLORING ADVANCED RTL CLOCK-GATING OPPORTUNITIES IN MICROPROCESSOR DESIGN

Krishnan Sundaresan, Aravind Oommen, Doug Meserve, Hemanga Das, Jaewon Oh, Jamil Mohd - *Oracle, Santa Clara, CA*

1U.4S ROBUST VARIATION-TOLERANT CLOCK ROUTING

Joseph Kozhaya, Phillip Restle, Haifeng Qian, Jan Feder - *IBM Corp., Yorktown Hts., NY*

Mehmet Yildiz - *IBM Corp., Austin, TX*

1U.5S RAPIDS: POST-ROUTING TIMING CLOSURE

Bill Dougherty - *IBM Corp., Pittsburgh, PA*

Michael Kazda - *IBM Corp., Hopewell Junction, NY*

1U.6S DESIGN FLOW QUALITY FEEDBACK USING PRODUCT PATH DELAY ANALYSIS

Lionel Riviere-Cazaux, Rick Woltenberg, Shweta Latawa - *Freescale Semiconductor, Inc., Austin, TX*

UT 2 POSTER SESSION

Tuesday, June 15 1:30 - 3:00pm

Rm: 2nd Floor Foyer Adjacent to 208AB

Moderator: **Sorin Dobre** - *Qualcomm, Inc., San Diego, CA*

Join us to view the Tuesday User Track Poster presentations. This poster session has approximately 40 posters on topics that span both front-end and back-end design, including posters from today's User Track sessions. The posters will offer an opportunity for personal interaction with EDA tool users from leading companies.

2U.1P USING STATISTICAL STATIC TIMING SIGN-OFF METHODOLOGY FOR VOLTAGE BINNING IN 45-NANOMETER

Xiaoyue Wang, Eric Foreman, Peter Habitz - *IBM Corp., Essex Junction, VT*

2U.2P SYNTHESIS VS. HAND DESIGN: A CASE STUDY ON AN ARITHMETIC DATAPATH DESIGN

Sreekanth Madgula, Subramaniam Maiyuran, Nowjand Attaie, K.K.Ram Ramakrishnan - *Intel Corp., Folsom, CA*

2U.3P IMPROVING POST-LAYOUT SIMULATION FLOW ACCURACY AND PRODUCTIVITY

Krishnakumar Sundaresan - *Synopsys, Inc., Pleasanton, CA*

2U.4P LAYOUT AUTOMATION IN A FULL-CUSTOM DESIGN ENVIRONMENT

Yoshiharu Kawamura - *Advanced Micro Devices, Inc., Sunnyvale, CA*

Sze Tom - *Advanced Micro Devices, Inc., Austin, TX*

2U.5P POST-LAYOUT VERIFICATION OF AMS DESIGNS AT 28NM

Hendrik Mau - *GLOBALFOUNDRIES, Dresden, Germany*

2U.6P SUPER-IP: HIERARCHICAL DESIGN, UPSIDE DOWN

Sreeram Chandrasekar, Hari Krishnamoorthy, Nithin SK, Kumud Singh - *Texas Instruments, Inc., Bangalore, India*

2U.7P CORRELATION AND PREDICTABILITY WITHIN A COMPLEX HIERARCHICAL DESIGN

Kevin Knapp - *Synopsys, Inc., Mountain View, CA*

2U.8P ANALYSIS OF POWER DELIVERY NETWORK OF MULTIPLE STACKED ASICS USING TSV AND MICRO-BUMPS

Damien Riquet, Lise Doyen, Jasmina Antonijevic - *STMicroelectronics, Crolles, France*

Aveek Sarkar, Nicolas Vialle - *Apache Design Solutions, Inc., San Jose, CA*

2U.9P AUTOMATICALLY MERGING TEST AND FUNCTIONAL MODE SDC FILES FOR PLACE AND ROUTE

Hans Kumar - *Broadcom Corp., San Jose, CA*

2U.10P ESD VERIFICATION AND ESD AWARE DESIGN OPTIMIZATION FOR COMPLEX SYSTEM-ON-A-CHIP DESIGN

Sorin Dobre**,** Amirali Shayan, Reza Jalilizeinali, Sreeker Dundigal, Siansuri Evan - *Qualcomm, Inc., San Diego, CA*

Khusro Sajid - *Qualcomm, Inc., Austin, TX*

2U.11P OPTIMIZING FOR POWER AND PERFORMANCE YIELD IN MOBILE APPLICATION PROCESSORS

Sreeram Chandrasekar, Sourav Banerjee, Ajoy Mandal, Mohit Sharma, Hari Krishnamoorthy - *Texas Instruments, Inc., Bangalore, India*

2U.12P DFM SCORING AND FIXING FROM BUSINESS GOAL TO TAPE-OUT

Lionel Riviere-Cazaux, Robert Boone - *Freescale Semiconductor, Inc., Austin, TX*

Fabio Melchiori, Domenico Ioparco - *STMicroelectronics, Agrate Brianza, Italy*

Matt Thompson - *Freescale Semiconductor, Inc., Austin, TX*

Philippe Sardin - *STMicroelectronics, Crolles, France*

2U.13P MINIMIZING DESIGN COMPLEXITY WITH POWER-OPTIMIZED PHYSICAL IP

Ken Brock, Lisa Minwell, **Brenda Westcott** - *Virage Logic Corp., Fremont, CA*

2U.14P AN INCREMENTAL, CORRECT BY CONSTRUCTION APPROACH OF ADDRESSING VIA DENSITY

Dibyendu Goswami, Swami Gangadharan - *Intel Corp., Bangalore, India*

Albert Holguin - *Intel Corp., Austin, TX*

2U.15P VERIFYING MULTI-PROTOCOL COMPLEX WIRELESS SOC USING OVM

Nilesh Ranpura - *eInfochips, Ahmedabad, India*

2U.16P HIGH SPEED MODELS FOR AUTOMOTIVE MICROCONTROLLERS: VERIFICATION OF THE TRICORE AUDO FUTURE TC1797 VIRTUAL PROTOTYPE

Jens Harnisch - *Infineon Technologies, Neubiberg, Germany*

Albrecht Mayer, Robert Schwencker, Prasanth Sasidharan - *Infineon Technologies, Munich, Germany*

Prasanna Kesavan - *Infineon Technologies, Noida, India*

Diamantino Goncalves - *Infineon Technologies, Bristol, United Kingdom*

Martin Schnieringer - *Synopsys, Inc., Mountain View, CA*

2U.17P HARD IP INTEGRATION - FROM ANALOG TO SOC INTEGRATION

James McCollum, Steven Klass - *SMSC, Phoenix, AZ*

2U.18P VERIFICATION OF MULTIPLE POWER SUPPLY DESIGNS USING POWER-AWARE SIMULATION

Osama Neiroukh - *Intel Corp., Haifa, Israel*

Aviv Barkai - *Intel Corp., Folsom, CA*

2U.19P VISUALIZING AND DOCUMENTING SYSTEMVERILOG CLASS-BASED TESTBENCHES WITH UML IN HIGH-RELIABILITY SPACE SYSTEMS

Peter LaFauci - *Mentor Graphics Corp., Cary, NC*

Brett Oliver, Jack Profumo, **Lucas Roosevelt** - *Honeywell International, Inc., Clearwater, FL*

2U.20P CIRCUIT ANALYSIS AND OPTIMIZATION UNDER MANUFACTURING VARIATIONS AND IMPACT ON DYNAMIC VOLTAGE SCALED SYSTEMS

Sachin Idgunji - *ARM Ltd., San Jose, CA*

Ayhan Mutlu - *Extreme DA Corp., Santa Clara, CA*

2U.21P AN OPEN DATABASE FOR THE OPEN VERIFICATION METHODOLOGY

Alberto Allara - *STMicroelectronics, Milano, Italy*

Sara Comai, Alessandro Alice - *Politecnico di Milano, Milano, Italy*

2U.22P USING SYSTEMVERILOG ASSERTIONS AND ZOCALO ZAZZ TO IMPROVE IP QUALITY

Eric Deal - *Cyclic Design, Austin, TX*

2U.23P HIGH-LEVEL SYNTHESIS OF A QUEUE MANAGER BLOCK - A CASE STUDY

Maneesh Soni, Akila Subramaniam - *Texas Instruments, Inc., Dallas, TX*

Per Edstrom, Steve Brown - *Cadence Design Systems, Inc.*

2U.24P DON'T FORGET THE HOLES IN THE BOX: UTILIZING EMBEDDED COMPONENTS FOR VERIFICATION

Ralph Martin - *Honeywell International, Inc., Tampa, FL*

Brett Oliver, Jack Profumo, **Lucas Roosevelt** - *Honeywell International, Inc., Clearwater, FL*

2U.25P NOVEL INFRASTRUCTURE FOR VERSATILE DESIGN VALIDATION METHODOLOGY WITH CUSTOMIZED HARDWARE PROTOTYPE SYSTEMS

Ying-Tsai Chang, Mike Shei, Ming-Yang Wang, Yu-Chin Hsu - *SpringSoft, Inc., San Jose, CA*

Howard Mao - *SpringSoft, Inc., Hsinchu City, Taiwan*

2U.26P SYSTEMC-BASED HIGH-LEVEL SYNTHESIS OF AN AVC/H.264 INTRA HDTV ENCODER

Takayuki Onishi, Koyo Nitta, Hiroe Iwasaki, Kazuto Kamikura - *Nippon Telegraph and Telephone Corp., Yokosuka, Japan*

2U.27P KEEPING HARDWARE, FIRMWARE, AND DOCUMENTATION FILES IN SYNC

Gary Stringham - *Gary Stringham & Assoc., LLC, Eagle, ID*

UT 3 Rm: 208AB

FRONT-END DESIGN EXPERIENCES

Tuesday, June 15 3:00 - 4:00pm

System-Level and Embedded

Moderator: **Benjamin Carrion Schafer** - NEC Corp., Kawasaki, Japan

This session covers some design challenges in today's SOC systems. Engineers from IMEC, Esteco s.r.l., and the University of Lugano describe how to trade off accuracy for speed using multiple simulators to explore the design space. Designers from University of Toulouse, Universiti Europeenne de Bretagne, and Thales Alenia Space present their Hardware/Software co-design experience for an onboard satellite navigation receiver. Engineers from STMicroelectronics share their unused flop deletion algorithm. Finally, Cypress engineers cover strategies to reduce hardware license purchasing and to reallocate licenses to newer features.

3U.1S PRACTICAL APPROACH FOR DESIGN SPACE EXPLORATIONS USING SIMULATORS AT MULTIPLE ABSTRACTION LEVELS

Prabhat Avasare, Geert Vanmeerbeeck - *IMEC, Leuven, Belgium*
Carlos Kavka - *Esteco s.r.l., Trieste, Italy*
Giovanni Mariani - *Univ. of Lugano, Lugano, Switzerland*

3U.2S HARDWARE/SOFTWARE CODESIGN EXPERIENCE FOR ONBOARD SATELLITE NAVIGATION RECEIVER

Arnaud Dion, Vincent Calmettes - *Univ. de Toulouse, Toulouse, France*
Emmanuel Boutillon - *Univ. Européenne de Bretagne, Lorient, France*
Emmanuel Liegeon - *Thales Group, Toulouse, France*

3U.3S UNUSED FLOP DELETION ALGORITHM LEADING TO IMPROVED TIME TO MARKET AND SOC COST SAVINGS

Arvind Kumar - *STMicroelectronics, Greater Noida, India*

3U.4S USING METRICS TO OPTIMIZE LICENSE AND HARDWARE PURCHASING AND REDUCE LICENSE EXPENSE

Jarrod Stykes - *Cypress Semiconductor Corp., San Jose, CA*

UT 4 Rm: 208AB

TAMING BACK-END VERIFICATION AND DFM

Tuesday, June 15 4:30 - 6:00pm

DFM and the Manufacturing Interface

Moderator: **Manuel d'Abreu** - *SanDisk Corp., Milpitas, CA*

The complexity of IC verification and test is skyrocketing due to the increased silicon and system complexity of advanced SOCs. In this session, six speakers from several major design companies will present their solutions to tame this problem. Solutions were found in robust DFT methodologies down to advanced thermal validation in 3-D chips. Other presenters focus on intelligent reduction of the massive amount of data and components. The final speaker will present various cost-effective ways to improve yield and manufacturability.

4U.1S 32NM IBM ASIC DESIGN FOR TEST METHODOLOGY

David Lackey - *IBM Corp., Essex Junction, VT*

4U.2S GLADIUS: AN ACCURATE METHOD FOR FAST PATH EXTRACTION IN MICROPROCESSOR DESIGN

Sujeeth Udipi, Sukhdeep Sidhu, **Walid Elgharbawy** - *Oracle, Santa Clara, CA*
Pravin Chandran - *Oracle, Sunnyvale, CA*

4U.3S 200X COMBINATIONAL SCAN COMPRESSION – ENABLER FOR TEST COST SCALING

Sarveswara Tammali, Rajesh Gottumukkala - *Texas Instruments, Inc., Bangalore, India*
Peter Wohl - *Synopsys, Inc., Williston, VT*
Frederic Neuveux - *Synopsys, Inc., Paris, France*

4U.4S USING CALIBRE PERC FOR FULL-CHIP DETECTION OF UNINTENTIONAL FORWARD-BIASED DIODES

Amir Grinshpon - *Freescale Semiconductor, Inc., Tel Aviv, Israel*
Adam Segoli Schubert - *Freescale Semiconductor, Inc., Herzelia, Israel*
Ziyang Lu - *Mentor Graphics Corp., Wilsonville, OR*

4U.5S A PRACTICAL APPROACH TO THERMAL MODELING AND VALIDATION OF 3-D ICs

Miroslav Cupak, Herman Oprins, Geert Van der Plas, Pol Marchal, Bart Vandevelde - *IMEC, Leuven, Belgium*
Adi Srinivasan, Edmund Cheng - *Gradient Design Automation, Inc., Santa Clara, CA*

4U.6S FAILURE ANALYSIS-DRIVEN DESIGN FOR MANUFACTURABILITY

Puneet Sharma, Chi-Min Yuan - *Freescale Semiconductor, Inc., Austin, TX*

UT 5 Rm: 208AB

CASE STUDIES IN FORMAL VERIFICATION

Wednesday, June 16 9:00 - 11:00am

Verification and Test

Moderator: **Srinath Atluri** - *Cisco Systems, Inc., San Jose, CA*

Today's verification tools have become very powerful due to a combination of simulation and formal techniques. Formal verification usually provides significant increases in productivity and quality. This session describes various techniques that were used to overcome challenges in formal verification. Several case studies are presented including the verification of a packet switch block, the Cortex A9 processor, three SOC designs from TI, analog-based design cells, at-speed clock verification, TriCore 1.6 microcontroller, and a complex transaction ID property on a coherence unit.

5U.1S LEVERAGING FORMAL TECHNIQUES FOR VERIFICATION OF PACKET-BASED DESIGNS

Balekudru Krishna, Anamaya Sullerey - *Chelsio Communications, Sunnyvale, CA*
Alok Jain - *Cadence Design Systems, Inc., Noida, India*

5U.2S A FORMAL POT-POURRI

Laurent Arditi - *ARM Ltd., Sophia Antipolis, France*

5U.3S AUTOMATED FORMAL VERIFICATION OF SPINNER-BASED SOC IO PAD FRAME LOGIC: CHALLENGES AND SOLUTION

Amit Roy, Supriya Bhattacharjee, Bijitendra Mittra - *Interra Systems, Inc., Bangalore, India*
Subir Roy - *Texas Instruments, Inc., Bangalore, India*

5U.4S LOGIC MODELING AND FORMAL EQUIVALENCE CHECKING OF ANALOG-BASED DESIGN

Moshe Emmer - *Intel Corp., Haifa, Israel*

5U.5S COMPLETE DFT RTL VERIFICATION USING FORMAL TECHNIQUES FOR COMPLEX SOCs

Arvind Jain, Edmond George, Subir Roy, Sundarrajan Subramanian - *Texas Instruments, Inc., Bangalore, India*
Lopamudra Sen - *Interra Systems, Inc., Bangalore, India*
Lokesh Babu - *Cadence Design Systems, Inc., Bangalore, India*

5U.6S FORMAL VERIFICATION OF MULTICYCLE OVERRIDES ON A GRAPHICS CHIP

Chunduri Mohan - *Intel Corp., Folsom, CA*
Vadivel Ramalingam, Bharathi V, Sreejith Pillai, Sacheendra Nath - *Intel Corp., Bangalore, India*

5U.7S USING A FORMAL PROPERTY CHECKER FOR SIMULATION COVERAGE CLOSURE

Tim Blackmore, David Halliwell, Philip Barker - *Infineon Technologies, Bristol, United Kingdom*
Kerstin Eder, **Naresh Ramaram** - *Univ. of Bristol, Bristol, United Kingdom*

5U.8S MAXIMIZING THE VALUE OF YOUR FORMAL RUN

George Plouffe - *Oracle, Santa Clara, CA*

UT 6

POSTER SESSION

Wednesday, June 16 1:30 - 2:30pm

Rm: 2nd Floor Foyer Adjacent to 208AB

Moderator: **Ben Chen** - *Cisco Systems, Inc., San Jose, CA*

This is the second User Track poster session at DAC. Join us in viewing approximately 40 posters on topics that span both front-end and back-end design, including the posters from today's User Track sessions.

6U.1P AUTOMATION FOR QUALITY IMPROVEMENTS

Chris Schalick - *GateRocket, Inc., Bedford, MA*

6U.2P AN EFFICIENT MULTI-VOLTAGE TIMING SIGN-OFF METHODOLOGY

Junichi Mano, **Kimihiro Ogawa** - *STARC, Yokohama, Japan*

6U.3P ECO METHODOLOGY FOR VERY HIGH FREQUENCY MICROPROCESSOR

Sumit Goswami, Srivatsa Srinath, Ravi Shekar, Anoop V - *Intel Corp., Bangalore, India*

6U.4P PHYSICAL DESIGN OF A STRUCTURED ASIC BASED ON ASIC DESIGN METHODOLOGY

Yanqing Ai, Steve C.L. Yuen, Thomas C.P. Chau, Sam M.H. Ho, Brian P.W. Chan, Oscar K.L. Lau, Kong-Pang Pun, Oliver C.S. Choy - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

Philip Leong - *The Univ. of Sydney, Sydney, Australia*

6U.5P DESIGN-CLOSURE OF MULTI-MILLION GATE CHIP USING FULL FLAT OPTIMIZATION TECHNOLOGY OF OLYMPUS–SOC

Pooja Mehra - *STMicroelectronics, Greater Noida, India*

Johann Meleard - *STMicroelectronics, Grenoble, France*

6U.6P FAST ESTIMATION AND MITIGATION OF SUBSTRATE NOISE IN EARLY DESIGN STAGE FOR LARGE MIXED-SIGNAL SOCs

Shi-Hao Chen, **Hsiung-Kai Chen**, **Albert Li** - *Global Unichip Corp., Hsinchu City, Taiwan*

Xiaopeng Dong, Vassilios Gerousis, Rose Li - *Cadence Design Systems, Inc., San Jose, CA*

Miles Zhang, Yanling Weng - *Cadence Design Systems, Inc., Shanghai, China*

6U.7P SUPERBLOCK: A METHOD FOR SYNTHESIZING LARGE HIGH PERFORMANCE DESIGNS WITHOUT HIERARCHY LIMITS

Murali Seshadri, Chris Mabee, Madhur Maheshwari, **Raj Varada** - *Intel Corp., Santa Clara, CA*

6U.8P A PRACTICAL STATISTICAL TIMING CHARACTERIZATION SYSTEM IN 40NM

Sam Lo, **Sridhar Premkumar**, Ray Shr, Aaron Barker, Ebrahim Khalily - *Oracle, Santa Clara, CA*

6U.9P LOW-POWER VERIFICATION FOR SOC USING FORMAL TECHNIQUES

Ayon Dey, Shailesh Ghotgalkar, Jacob Joseph, Shekhar Sharma - *Texas Instruments, Inc., Bangalore, India*

6U.10P REDUCING DYNAMIC POWER WITH GATE-LEVEL CLOCK-GATING OPTIMIZATION

Subrangshu Das, Mohit Sharma, Sarveswara Tammali, Rajesh Gottumukkala - *Texas Instruments, Inc., Bangalore, India*

Aishwarya Singh - *Indian School of Business, Bangalore, India*

Amit Singh - *Azuro, Inc., Bangalore, India*

6U.11P ANALOG DESIGN AUTOMATION: AN INDUSTRIAL PERSPECTIVE

Mohamed Dessouky - *Mentor Graphics Corp., Cairo, Egypt*

6U.12P GRAPH-BASED ALGORITHMIC STIMULUS GENERATION TOOL REDUCES TIME TO COVERAGE CLOSURE VERIFYING 802.11* DEVICES

Chandramouli Ganapathy - *Atheros Communications, Inc., Sunnyvale, CA*

Jay O'Donnell - *Mentor Graphics Corp., Cary, NC*

6U.13P A CASE STUDY INVOLVING AN OVM-BASED ESL VERIFICATION FLOW

Jen-Chieh Yeh - *Industrial Technology Research Institute, Hsinchu, Taiwan*

Joerg Simon - *Cadence Design Systems, Inc., Feldkirchen, Germany*

6U.14P EXPERIENCES IN ADDRESSING CRITICAL POWER MANAGEMENT VERIFICATION ISSUES IN LOW-POWER DESIGNS

Bhanu Kapoor - *Mimasic, Richardson, TX*

Prapanna Tiwari - *Synopsys, Inc., Chandler, AZ*

John Goodenough - *ARM Ltd., San Jose, CA*

Amit Kumar - *CSR, San Jose, CA*

6U.15P SEQUENTIAL DISTANCE ANALYSIS: A METRIC FOR ASSERTION COVERAGE

Xiaolin Chen - *Synopsys, Inc., Mountain View, CA*

Thomas Thatcher - *Oracle Corp, Santa Clara, CA*

Abhishek Muchandikar - *Synopsys, Inc., Bangalore, India*

Surrendra Dudani - *Synopsys, Inc., Marlboro, MA*

6U.16P GREEN FLASH—DESIGN AND EMULATE A LOW-POWER CPU FOR A NEW CLIMATE-MODELING SUPERCOMPUTER

David Donofrio, John Shalf - *Lawrence Berkeley National Lab, Berkeley, CA*

John Wawrzynek - *Univ. of California, Berkeley, CA*

6U.17P A TOOL TO AID TO GENERATE ADAPTIVE MBIST TEST VECTORS

Weili Wang - *Cisco Systems, Inc., San Jose, CA*

6U.18P AN EFFICIENT METHOD OF TIMING GENERATION FOR ANALOG IP IN MIXED-SIGNAL INTEGRATION

Wells Jong, Mexx Lin, Ean Tzeng, David Wu, Joseph Chang, Wenn Lo - *Faraday Technology Corp., Hsinchu City, Taiwan*

6U.19P LET'S SEE YOU SIMULATE THIS! USING FORMAL TO VERIFY A SYNTHESIZABLE TESTBENCH CONSTRAINT SOLVER

Matthew Hsu - *Matthew A. Hsu Consulting, San Jose, CA*

6U.20P FOR BETTER RESULTS: ESTABLISH CLOSER TIES BETWEEN FORMAL VERIFICATION AND SIMULATION TEAMS

Thomas Thatcher - *Oracle, Santa Clara, CA*

Lawrence Loh, Holly Stump - *Jasper Design Automation, Inc., Mountain View, CA*

6U.21P CLOCK DOMAIN CROSSING VERIFICATION SIGN-OFF IN A MULTI-MILLION GATE SOC

Ayon Dey , Shailesh Ghotgalkar, Gokulakrishnan Manoharan - *Texas Instruments, Inc., Bangalore, India*

Paras Jain - *Atrenta, Inc., Noida, India*

Namit Gupta - *Atrenta, Inc., San Jose, CA*

UT 7 CORNERED: DEALING WITH VARIABILITY

Rm: 208AB

Wednesday, June 16 3:00 - 4:00pm

Interconnect and Reliability

Moderator: **Bryan Heard** - *QThink, Inc., San Diego, CA*

The art of modern 22nm subwavelength lithography has been compared to painting Mona Lisa with a 1-inch brush. At the same time oxide thickness and most other device dimensions are measured in just a few hands full of atoms. This physical reality inevitably results in significant design variability, both systematic and random. The number of traditional PVT corners is exploding, making it less adequate in dealing with this problem. This session presents recent industrial advances in Statistical Static Timing as an alternative to the traditional multi-corner approach.

7U.1S A NEW GENERATION STATIC STATISTICAL TIMING ANALYSIS (SSTA) BASED DESIGN FLOW FOR 40nm AND 28nm CMOS TECHNOLOGY

Terumi Yoshimura, Toshikatsu Hosono - *Fujitsu VLSI Ltd., Kasugai, Japan*
Jun Li, Janet Wang - *Anova-Solutions, Inc., Santa Clara, CA*

7U.2S MANAGING VARIATION AT ADVANCED NODES IN TIMING VERIFICATION

Tong Xiao, Ebrahim Khalily, Aaron Barker, Bogdan Tutuianu, Rob Mains - *Oracle, Santa Clara, CA*

7U.3S ENABLEMENT OF STATISTICAL STATIC TIMING SIGN-OFF METHODOLOGY USING INDUSTRY STANDARD LIBERTY TIMING MODELS FOR 32nm

Dileep Netrabile, **Eric Foreman**, Nathan Buck - *IBM Corp., Essex Junction, VT*

7U.4S A NEW TIMING CLOSURE METHODOLOGY FOR AN SOC WITH MULTIPLE ON-CHIP REGULATORS

Tatsuo Shiozawa, Tetsuya Fujita, Hiroyuki Hara, Shuuji Matsumoto, Keiko Seki-Fukuda, Toshio Fujisawa, Masanori Kuwahara, Toshitada Saito, Yasuo Unekawa, Mototsugu Hamada - *Toshiba Corp., Kawasaki, Japan*

UT 8 FRONT-END TESTING AND VERIFICATION

Rm: 208AB

Wednesday, June 16 4:30 - 6:00pm

System-level and Embedded

Moderator: **Tor Jeremiassen** - *Texas Instruments, Inc., Houston, TX*

Complex SOC architectures impose difficult verification and test challenges. IBM presents a novel approach for generating test cases that exercise accelerators at the system level. Engineers from Marvell and EVE address high-performance HW/SW co-verification by migrating simulation to emulation. Marvell also shares their advanced delay modeling techniques to generate complex, timing-centric test scenarios with delay-space test coverage. Intel presents a methodology to deliver an efficient pre-RTL abstract functional model. Mentor describes an Interoperability library to bridge the gap between OVM and VMM. Finally, Synopsys and AMD present a customized coverage grading solution to improve the standard and flow at AMD.

8U.1S HYBRID SYSTEM-LEVEL TEST GENERATION APPROACH FOR HETEROGENEOUS SYSTEMS

Alex Goryachev, Ronny Morad, **Wisam Kadry** - *IBM Corp., Haifa, Israel*

8U.2S MIGRATING HW/SW CO-VERIFICATION PLATFORMS FROM SIMULATOR TO EMULATOR

Alicia Strang, Robert Carden - *Marvell Semiconductor, Inc., Aliso Viejo, CA*
Ronald Choi - *EVE-USA, Inc., Toronto, ON, Canada*

8U.3S DIAGNOSIS OF COMPLEX DESIGN/ARCHITECTURE PROBLEMS USING BFMs WITH ADVANCED DELAY MODELING

Ravi Kalyanaraman, Kumaril Bhatt, Nikhil Mungre - *Marvell Semiconductor, Inc., Santa Clara, CA*

8U.4S ABSTRACT FUNCTIONAL MODEL-BASED COVERAGE AND TEST GENERATION

Adriana Wolffberg, Gila Kamhi, Simaan Nassar, Tali Levy - *Intel Corp., Haifa, Israel*
Raj Rajput - *Intel Corp., Bangalore, India*

8U.5S REUSE IN THE REAL WORLD - PROVING THE ACCELLERA VIP INTEROPERABILITY KIT

Manoj Manu - *Mentor Graphics Corp., Noida, India*
Ashish Kumar - *Mentor Graphics Corp., Bangalore, India*
Adam Erickson - *Mentor Graphics Corp., Waltham, MA*

8U.6S QUICKGRADE: AN EFFICIENT ALGORITHM FOR MANAGING COVERAGE GRADING IN COMPLEX MULTICORE MICROPROCESSOR ENVIRONMENTS

James Young, Michael Sanders - *Advanced Micro Devices, Inc., Austin, TX*
Paul Graykowski - *Synopsys, Inc., Austin, TX*
Vernon Lee - *Synopsys, Inc., Mountain View, CA*

UT 9 POWER DELIVERY FROM PACKAGE TO CHIP

Rm: 208AB

Thursday, June 17 9:00 - 11:00am

Low-Power Design

Moderator: **Raj Varada** - *Intel Corp., Santa Clara, CA*

Power optimization and verification is one of the most challenging tasks that SOC design teams face. With each technology node the supply voltage is scaled down to keep dynamic power consumption under control. The resulting high current and smaller threshold voltages significantly reduce the design margins. In addition, sub-threshold leakage increases. The power infrastructure must be carefully designed and dimensioned on the chip, in the package and on the PCB. In this session, presenters from leading design companies will present various innovative solutions for the design and analysis of power distribution networks from various angles.

9U.1S PACKAGE/PCB AWARE ON-DIE POWER GRID NOISE ANALYSIS

Sorin Dobre, Amirali Shayan, Mikhail Popovich, Kevin Bowles, Xiaoming Chen, Christopher Pan - *Qualcomm, Inc., San Diego, CA*

9U.2S POWER SHAPING METHODOLOGY FOR SUPPLY NOISE AND EMI REDUCTION

Fabio Campi - *STMicroelectronics, Bologna, Italy*
Tobias Bjerregaard, Mikkel Stensgaard - *Teklatech A/S, Copenhagen, Denmark*
Davide Pandini - *STMicroelectronics, Agrate Brianza, Italy*

9U.3S POWER DELIVERY NETWORK DESIGN AND ANALYSIS

Erhan Ergin - *Advanced Micro Devices, Inc., South Orange, NJ*
Julius Din - *Advanced Micro Devices, Inc., Sunnyvale, CA*
David Chakkuthara, Tony Todesco - *Advanced Micro Devices, Inc., Austin, TX*
Mark Frankovich, Fei Guo, Gabriel Wong, Royston Sequeira, Silqun Leung, Thad Yogarasa - *Advanced Micro Devices, Inc., Markham, ON, Canada*

9U.4S POWER NOISE MITIGATION STRATEGY FROM RLT PERSPECTIVE ON MTCMOS DESIGN

Leekee Yong, CheeSiong Lee - *Intel Corp., Penang, Malaysia*
Fern Nee Tan - *Intel Corp., Bayan Lepas, Malaysia*

9U.5S A PRACTICAL FRAMEWORK FOR STATISTICAL LEAKAGE ESTIMATION

Kyung-Tae Do, Jung Yun Choi, Seokhoon Kim, Hyein Lee, Hyo-Sig Won, Kyu-Myung Choi - *Samsung, Yongin-City, Republic of Korea*

9U.6S AN ACCURATE AND EFFICIENT SSO/SSN SIMULATION METHODOLOGY FOR 45NM LPDDR I/O INTERFACE

Rajen Murugan, **Souvik Mukherjee** - *Texas Instruments, Inc., Dallas, TX*
Vinayakam Subramanian - *Apache Design Solutions, Inc., Dallas, TX*
Ji Zheng - *Apache Design Solutions, Inc., San Jose, CA*

9U.7S A COMPREHENSIVE ESD PROTECTION DESIGN FLOW UTILIZING SUITE OF ESD VERIFICATION TOOLS IN ADVANCED TECHNOLOGIES

Mujahid Muhammad, Robert Gauthier, Junjun Li, Ahmed Ginawi, James Montstream, Souvick Mitra, Amol Joshi, Nicholas Palmer, Brian Hulse - *IBM Corp., Essex Junction, VT*
Karen Henderson - *IBM Corp., Westford, MA*

9U.8S RINGING IN AND OUT: AUTOMATED CREATION OF THE SOC I/O RING

Ayon Dey - *Texas Instruments, Inc., Bangalore, India*
Sean Boylan, David Murray - *Duolog Technologies Ltd., Galway, Ireland*
Bob Maaraoui - *Texas Instruments, Inc., Dallas, TX*

UT 10 POSTER SESSION

Thursday, June 17 1:30 - 2:30

Rm: 2nd Floor Foyer Adjacent to 208AB

Moderator: **Alicia Strang** - *Marvell Semiconductor, Inc., Aliso Viejo, CA*

Join us once again for the third User Track Poster Session at DAC. This session offers approximately 40 poster presentations spanning both front-end and back-end design, including the posters from today's User Track sessions.

10U.1P AN RTL APPROACH TO MEMORY-BIST INSERTION WITH PROPRIETARY ARCHITECTURES

Marcello Raimondi, Alberto Carava - *STMicroelectronics, Milano, Italy*

Frederic Grandvaux - *STMicroelectronics, Crolles, France*

10U.2P 32nm LIBRARY DESIGN TECHNOLOGY CO-OPTIMIZATION THROUGH DESIGN FOR MANUFACTURABILITY TOOLS

Tina Wagner, Ioana Graur - *IBM Corp., Hopewell Jct., NY*

Kuang-Kuo Lin, - *GLOBALFOUNDRIES, Malpitas, CA*

Seungweon Paek, Daehyun Jang, Joohyun Park - *Samsung, Yong-In, Republic of Korea*

NanShu Chen, Shyue-Fong Quek, Paul Soh, Xiao-Yong Wang - *GLOBALFOUNDRIES, Singapore, Singapore*

Marlin Frederick Jr., Dave Clark- *ARM Ltd., Austin, TX*

10U.3P FIXING HOLD IN TEST SHIFT MODE WITHOUT USING BUFFERS

Sachin Mathur, **Shalini Dhami** - *STMicroelectronics, New Delhi, India*

10U.4P A CASE STUDY: APPLYING SEMI-CUSTOM DESIGN FLOW TO ADDRESS ROUTING CHALLENGE

Jun Xu, **Ge Zhang**, Jiangmei Wang, Weiwu Hu - *Chinese Academy of Sciences, Beijing, China*

10U.5P TIMING CRITICAL PROCESSOR DESIGN CLOSURE

Deepti Miyan, Ashish Khurana - *STMicroelectronics, Greater Noida, India*

10U.6P AUTOMATIC PRE - AND POST-SILICON FUNCTIONAL ECO FLOW

Ganesh Prabhu Chandrasekaran, Bhanu Prakash - *STMicroelectronics, Greater Noida, India*

10U.7P TIMING MARGIN REDUCTION WITH STATISTICAL CHARACTERIZATION FOR SRAM CELL

Keiichi Morikawa, Fumihiro Minami - *STARC, Yokohama, Tokyo, Japan*

Yuuki Sato - *Marubeni Information Systems Co., Ltd., Japan*

Ken Tseng - *Altos Design Automation, San Jose, CA*

10U.8P A NOVEL FREQUENCY DOMAIN NOISE ANALYSIS THROUGH DIFFERENT POWER DOMAINS FOR LARGE SOC DESIGNS

Genichi Tanaka, Fumitaka Kurose, Yojiro Uchimura, Yoshifumi Sasaki, Yuji Ishioka - *Renesas Electronics Corp., Itami, Japan*

10U.9P CHIP ASSEMBLY FLOW: QUICK AND EASY WAY TO REDUCE TIMING ANALYSIS CYCLE TIME

Sachin Mathur, Shalini Dhami - *STMicroelectronics, New Delhi, India*

10U.10P INCREMENTAL SMALL DELAY DEFECT METHODOLOGY

Akhil Garg, Swapnil Bahl - *STMicroelectronics, Noida, India*

Roberto Mattiuzzo, Saverio Graniello, Paolo Cavenaghi - *STMicroelectronics, Agrate Brianza, Italy*

10U.11P POWER DEVICE ANALYSIS IN DESIGN FLOW FOR SMART POWER TECHNOLOGIES

Luciana Paciaroni, **Antonio Bogani**, Paolo Cacciagrano, Marco Verga, Giorgio Ferre` - *STMicroelectronics, Milan, Italy*

Maxim Ershov, Yuri Feinberg, Andrei Tcherniaev - *Silicon Frontline Inc., Campbell, CA*

10U.12P CORRELATING PREDICTED AND ACTUAL POWER IN A 90nm ASIC POWER ISLAND

Jeff Geneser - *Rockwell Collins, Inc., Cedar Rapids, IA*

10U.13P PUSHING THE TOOLS ENVELOPE WITH A RAD HARD MEGACHIP

AJ Kleinosowski, **Jon Ballast**, Bryan Buchanan, Tuan Dao, Duncan Lam, Roderick Mercer, Charles Neathery, Michael Smith - *Boeing, Seattle, WA*

10U.14P SHAPES-BASED PROCESS MIGRATION AND DFM OPTIMIZATION USING MINIMUM PERTURBATION COMPACTION

Ryan Bazinet - *IBM Corp., East Fishkill, NY*

Veit Gernhoefer - *IBM Corp., Boeblingen, Germany*

Michael Gray, Matthew Guzowski, Kevin McCullen - *IBM Corp., Essex Junction, VT*

Rani Narayan - *IBM Corp., San Jose, CA*

Robert Walker - *IBM Corp., Essex, VT*

Xin Yuan - *IBM Corp., Hopewell Junction, NY*

10U.15P ACCELERATING DV CLOSURE THROUGH COVERAGE ADAPTIVE TECHNIQUES FOR OPTIMAL TEST-SUITE GENERATION

Ashish Chandra, Chaitanya Vaddadi, Harsh Setia, Vasant Vaghamshi, Sai Komaravelli - *Texas Instruments, Inc., Bangalore, India*

10U.16P A NOVEL APPROACH TO COMPLEX INTERRUPT CONTROLLER VERIFICATION

Ashish Chandra - *Texas Instruments, Inc., Bangalore, India*

10U.17P RTL POWER OPTIMIZATION IN SEQUENTIAL ANALYSIS PLATFORMS

Jairam Sukumar, **Subrangshu Das**, Mohit Sharma, Udayakumar H, Jagdish Rao - *Texas Instruments, Inc., Bangalore, India*

Amit Goldie, Abhishek Ranjan - *Calypto Design Systems, Inc., Noida, India*

10U.18P SELECTION AND INTEGRATION OF A SIGNAL PROCESSING PACKAGE FOR A SYSTEMVERILOG/VMM VERIFICATION ENVIRONMENT

Ron Shipp - *Synopsys, Inc., Austin, TX*

Wes Kirk, Matt Spaethe - *Motorola, Inc., Fort Worth, TX*

10U.19P AUTOMATIC LBIST DIAGNOSIS FLOW UNDER BOARD/93K TEST ENVIRONMENT USING ATPG TOOL AND ASSET

Zhiyuan Wang, Huai Li, Xinli Gu, **Toai Vo** - *Cisco Systems, Inc., San Jose, CA*

10U.20P EARLY SILICON VIRTUAL PROTOTYPING DESIGN METHODOLOGY FOR SOC DESIGN

Kwang-Hyun Cho, Woo-Joo Kim, Hyung-Il Jeon, Byeong Min, Kyu-Myung Choi - *Samsung, Yongin-City, Republic of Korea*

Jeong-Hwan Yoon, Jay Lee, Sung-Hwan Oh - *Entasys Design Inc., Seoul, Republic of Korea*

10U.21P CONSTRUCTING ELECTRONIC SYSTEM-LEVEL MODELS USING SIMULINK

Cheng-Chien Chen - *Faraday Technology Corp., Hsinchu City, Taiwan*

10U.22P CONFIGURABLE SUB-SYSTEM VERIFICATION USING PROPERTY BASED FORMAL METHODS

Supriya Bhattacharjee, Bijitendra Mittra - *Interra Systems, Inc., Bangalore, India*

Subir Roy - *Texas Instruments, Inc., Bangalore, India*

10U.23P BUG HUNTING METHODOLOGY USING SEMI-FORMAL VERIFICATION TECHNIQUES

Bijitendra Mittra, Deepanjan Roy - *Interra Systems, Inc., Bangalore, India*

Subir Roy - *Texas Instruments, Inc., Bangalore, India*

Lokesh Babu P - *Cadence Design Systems, Inc., Bangalore, India*

10U.24P A SMART DEBUGGING STRATEGY FOR BILLION-GATE SOCs

Namdo Kim, Junhyuk Park, Byeong Min, K.M. Choi - *Samsung, Yongin-City, Republic of Korea*

Kyuho Shim, Seiyang Yang - *Pusan Univ., Busan, Republic of Korea*

10U.25P A METHODOLOGY FOR AUTOMATIC GENERATION OF REGISTER BANK RTL, RELATED VERIFICATION ENVIRONMENT AND FIRMWARE HEADERS

Saurin Patel, Mukesh Chopra, **Bhawna Chopra** - *STMicroelectronics, Greater Noida, India*

10U.26P INTERCONNECTION BIST METHODOLOGY FOR MEMORY KGD IN SIP

Yusen Ou, Yuwei Chen, Yu-Wen Tsai, **Wells Jong** - *Faraday Technology Corp., Hsinchu City, Taiwan*

10U.27P UTILIZING ASSERTION SYNTHESIS TO ACHIEVE AN AUTOMATED ASSERTION-BASED VERIFICATION METHODOLOGY FOR A COMPLEX GRAPHICS CHIPS DESIGNS

Prosenjit Chatterjee, **Saad Godil**, Peter Nelson - *NVIDIA Corp., Santa Clara, CA*

Yuan Lu - *NextOp Software, Inc., Santa Clara, CA*

UT 11 Rm: 208AB USER TRACK PANEL: WHAT WILL MAKE YOUR NEXT DESIGN EXPERIENCE A MUCH BETTER ONE?

Thursday, June 17 2:30 - 4:00pm

Moderator: **Juan-Antonio Caraballo** - *IBM Corp., San Mateo, CA*
Organizer: **Thomas Harms** - *Infineon Technologies AG, Munich, Germany*

Speakers:
Ruud Haring - *IBM Corp., Yorktown Hts., NY*
James You - *Broadcom Corp., Irvine, CA*
Reynold D'sa - *Intel Corp., Santa Clara, CA*
Derek Urbaniak - *Oracle, Austin, TX*
Guntram Wolski - *Cisco Systems, Inc., San Jose, CA*

Top-designers and design engineering managers will present this top wish list to make their next (or even current) design a much better design experience. They will not focus on pie-in-the-sky research topics, but describe down to earth challenges designers face in getting their designs out the door. The panelists will use their data and experiences to substantiate their wish lists and address the main question: What needs to change in the design flows and design tools to improve Time-to-Market (TTM) and design quality? Joint presentation with Session 43.

UT USER TRACK BEST POSTER AWARDS

Thursday, June 17 4:00pm

RM: 208AB

UT 12 Rm: 208AB ADVANCES IN SYSTEM-LEVEL DESIGN AND SYNTHESIS

Thursday, June 17 4:30 - 6:00pm

System-Level and Embedded

Moderator: **David Black** - *XtremeEDA Corp., Austin, TX*

This session highlights design practices using high-level synthesis and SystemC/TLM. Designers at TI and Interra demonstrate how architectural exploration aids in designing a complex multi-media subsystem. NEC demonstrates using high-level synthesis to design a complex IP. Engineers from LG Electronics describe how to use ESL tools for SOC optimization. TI presents an approach to integrate software-debugging and user command semantics using a SystemC-based virtual platform. Cadence presents a TLM-driven methodology and case study to bridge the gap between virtual platform models and synthesizable SystemC models. Finally, Intel demonstrates how to visualize/debug TLM-2.0 AT transactions using SCV transaction recording.

12U.1S SYSTEMATIC ARCHITECTURE EXPLORATION THROUGH HIGH-LEVEL SYNTHESIS
Raj Mitra, Mahesh Mehendale - *Texas Instruments, Inc., Bangalore, India*
Praveen Tiwari - *Interra Systems, Inc., Bangalore, India*

12U.2S HIGH-LEVEL SYNTHESIS DESIGN SPACE EXPLORATION
Benjamin Carrion Schafer, Kazutoshi Wakabayashi - *NEC Corp., Kawasaki, Japan*

12U.3S A TWO-PHASED MULTI-MEDIA SOC DESIGN OPTIMIZATION USING ESL TOOLS
Hoon Oh, Youngkil Park, Byungchul Hong, Chulho Shin, Derek Ko - *LG Electronics, Seoul, Republic of Korea*

12U.4S INTEGRATING SOFTWARE-DEBUGGER ON A SYSTEMC-BASED VIRTUAL PLATFORM
Nizamudheen Ahmed, Gulur Dwarakanath Nagendra - *Texas Instruments, Inc., Bangalore, India*

12U.5S DEVELOPING SYNTHESIZABLE IP MODULES FROM TLM 2.0 DESCRIPTIONS - A TDIP METHODOLOGY CASE STUDY
Christian Sauer - *Cadence Design Systems, Inc., Munich, Germany*
Felice Balarin - *Cadence Design Systems, Inc., San Jose, CA*

12U.6S SCV TRANSACTION RECORDING AND APPLICATION TO TLM-2.0 AT STYLE PERFORMANCE MODELING
Zhu Zhou, Atul Kwatra - *Intel Corp., Chandler, AZ*
Trevor Wieman - *Intel Corp., Colorado Springs, CO*

TUTORIALS

T — ESL DESIGN AND VIRTUAL PROTOTYPING OF MPSOCs

Rm: 209AB

Monday, June 14 9:00am - 5:00pm

System-Level and Embedded

Continental Breakfast: 7:30am and Lunch: 11:30am - 204C
IEEE/ACM Member $300 Non-Member $400 Student IEEE/ACM Member $200 Student Non-Member $400

Organizers: **Philippe Coussy** - *Univ. de Bretagne, Cedex, France*
Alain Greiner - *Univ. Pierre et Marie Curie, Paris, France*

Complex embedded systems need new ESL level tools in order to raise the specification abstraction level. Platform based virtual prototyping offers the prospect of improving both the productivity and the quality of digital systems development. Designing at higher levels of abstraction is an obvious way as it allows to cope with the system design complexity, to verify earlier in the design process and to increase code reuse.

The tutorial will provide a comprehensive introduction to ESL design and Virtual Prototyping. Basic definitions, key concepts and typical design flows, will be presented. Industrial case studies using Virtual Prototyping will be detailed. The aim is for attendees to learn about ESL design techniques (platform based modeling, TLM, virtual prototyping, software synthesis, high-level synthesis, design space exploration…). They can use immediately an available platform included in a live CD that will be distributed to all participants. Finally, the tutorial will give a view of the directions the industry is taking for the longer term. We will examine the use and impact of ESL approach on the design process, from specification to implementation.

Speakers:
Philipe Coussy - *Univ. de Bretagne, Cedex, France*
Alain Greiner - *Univ. Pierre et Marie Curie, Paris, France*
Huy-Nam Nguyen - *Bull S.A.S., Fresnes, France*
Laurent Maillet-Contoz - *STMicroelectronics, Grenoble, France*
Frederic Petrot - *TIMA Labs, Grenoble, France*
Nicolas Pouillon - *Univ. Pierre et Marie Curie, Paris, France*

T — LOW-POWER FROM A TO Z

Rm: 210CD

Monday, June 14 9:00am - 5:00pm

Low-Power Design

Continental Breakfast: 7:30am and Lunch: 11:30am - 204C
IEEE/ACM Member $300 Non-Member $400 Student IEEE/ACM Member $200 Student Non-Member $400

Organizer: **Dennis Sylvester** - *Univ. of Michigan, Ann Arbor, MI*

Reducing power consumption has become the primary goal of integrated circuit designers today. This tutorial is aimed at providing a comprehensive look at how low-power design permeates all levels of the design process. Attendees will see how power is addressed from the technology level up to system-level design, including testability issues.

First, technological issues related to low-power design are discussed. Important concepts in designing for low-power are introduced, including clock/power gating, voltage islands, level shifting, multi-threshold, channel length biasing, stacking, and well biasing. More advanced power concepts such as dynamic voltage and frequency scaling, adaptive scaling, and memory voltage scaling limitations are then discussed. Library characterization is greatly complicated by many low-power techniques, for instance inverted temperature dependencies arise at low supply voltages observed in DVFS systems – these issues will also be covered.

After this, the unified power format (UPF) is introduced with a concrete discussion on how to write UPF for a design with many common low-power design techniques in place. An example design is walked through the flow from verification to implementation to sign-off.

Power management has recently become a pain point for manufacturing test. There are four major areas of low-power test to be addressed, including 1) power-aware design-for-test (DFT), 2) generation of power-aware test models, 3) ATPG and diagnosis for low-power structures such as isolation logic and level shifters, and 4) power reduction during test applications. The use of power specifications to improve automation in a low power flow will also be described with examples and results.

The tutorial concludes with two design case studies from leading SOC designers. Designing products with next generation process technology requires meaningful power estimation be done long before bottom-up data is available to enable product tradeoffs. This tutorial will describe an industrial view on doing this by 1) developing high level models of an expected design even before RTL is available, 2) developing forward looking energy cost functions for them in the new process technology, 3) increasing the granularity of the model to match the physical implementation, and 4) leveraging the model to expand IP coverage. Further discussion will describe how a low-power design process can iterate on transistor technology, power management granularity and algorithms, and product planning to balance features across the product.

Finally, an SOC targeting a medical application is described that achieves ultra-low-power operation by employing novel circuit design, system architecture, and SOC implementation methodologies. The tutorial describes challenges and solutions involved in design, library characterization, EDA tool flow, and methodology during this design.

Speakers:
Robert Aitken - *ARM Ltd., San Jose, CA*
Vivek Chickermane - *Cadence Design Systems, Inc., Endicott, NY*
Steve Curtis - *Intel Corp., Austin, TX*
Godwin Maben - *Synopsys, Inc., Mountain View, CA*
Srinivasa R. Sridhara - *Texas Instruments, Inc., Dallas, TX*

TUTORIALS

T — SYSTEMC FOR HOLISTIC SYSTEM DESIGN WITH DIGITAL HARDWARE, ANALOG HARDWARE, AND SOFTWARE

Rm: 210AB

Friday, June 18 8:30am - 12:30pm

System-Level and Embedded

Continental Breakfast: 7:30am - 204AB
IEEE/ACM Member $180 Non-Member $240 Student IEEE/ACM Member $120 Student Non-Member $240

Organizer: **Jürgen Teich** - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*

Embedded System Design in the era of Cyber-Physical Systems (CPS) is becoming a multi-disciplinary task which demands for system description languages and methodologies suitable to express and analyze different aspects of a design. Today, SystemC is the de-facto language standard to describe digital systems. One of its strongest contributions is SystemC's ability to model the interoperability of hardware and software components. Besides the modeling of digital systems, the SystemC AMS language standard has been evolved to include modeling and simulation of analog, continuous-time systems, allowing even to handle the more and more tighter interaction with the system's analog parts. The objective is to use SystemC as modeling language for multi-domain systems, where both electrical and non-electrical domains come together.

In this tutorial, we will cover the key concepts and state-of-the-art methodologies for SystemC-based system development processes. A special emphasis is put on the interoperability of different domains, i.e., hardware, software, and analog. We will present an overview of the state-of-the-art for a wide range of aspects including important topics such as executable specification, heterogeneous multi-processor SOC design, hardware-dependent software optimization, hardware/software co-verification, and analog, continuous-time system modeling. Industrial use cases will be used to illustrate the benefits from using and combining these methodologies based on SystemC's ability to describe multi-domain systems.

This tutorial is targeted towards system, embedded software, and hardware developers, and managers of system designers, and verification engineers, who use or are interested to understand the overall picture of today's system-level design, its challenges and available solutions.

Speakers:
Martin Barnasconi - *NXP Semiconductors, Eindhoven, The Netherlands*
Wolfgang Ecker - *Infineon Technologies AG, Neubiberg, Germany*
Karsten Einwich - *Fraunhofer IIS, Dresden, Germany*
Christian Haubelt - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*
Grant Martin - *Tensilica, Inc., Santa Clara, CA*

T — 3-D: NEW DIMENSIONS IN IC DESIGN

Rm: 210CD

Friday, June 18 9:00am - 5:00pm

General Interest

Continental Breakfast: 7:30am and Lunch: 11:30am - 204AB
IEEE/ACM Member $300 Non-Member $400 Student IEEE/ACM Member $200 Student Non-Member $400

Organizer: **Yuan Xie** - *Pennsylvania State Univ., University Park, PA*

3-D integration technology offers an attractive solution to meet the challenges of high performance, differentiated technology integration, and smaller form factor in future complex microprocessor and System-On-a-Chip (SOC) design. Adding the third dimension to design opens up new opportunities for EDA tools and design/architectural techniques to fully explore new approaches and address the challenges of 3-D integration. The goal of this tutorial is to provide an overview of the technology, the corresponding design challenges, and existing solutions to overcome these challenges. This tutorial brings leading 3-D IC experts in both industry and academia, and will provide a comprehensive coverage of various key topics in 3-D IC design.

Speakers:
David Atienza - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*
Tanay Karnik - *Intel Corp., Hillsboro, OR*
Paul Marchal - *IMEC, Heverlee, Belgium*
Ruchir Puri - *IBM Corp., Yorktown Hts., NY*
Yuan Xie - *Pennsylvania State Univ., University Park, PA*

T — HOW TO WRITE BETTER SOFTWARE

Rm: 209AB

Friday, June 18 9:00am - 5:00pm

General Interest

Continental Breakfast: 7:30am and Lunch: 11:30am - 204AB
IEEE/ACM Member $300 Non-Member $400 Student IEEE/ACM Member $200 Student Non-Member $400

Organizer: **Karen Rosengren** - *IBM Corp., Round Rock, TX*

EDA software is essential for handling nanometer-scale device geometries and increasing system complexities. Despite the fact that EDA professionals and students devote significant effort to understand technology and hardware, a major portion of their actual time is spent implementing complex software systems. Writing EDA software is also made more complex by the need to run on heavily threaded and multicore platforms. Similar challenges are faced by hardware developers who write embedded software for increasingly complex embedded systems. Do you have the software engineering skills to design these complex software systems?

To aid you, DAC has invited two industry experts with extensive training experience to teach you about state-of-the-art software development techniques. This presentation will appeal to anyone involved in software development: EDA developers, researchers, students, firmware engineers and application engineers.

This intensive full-day tutorial is a condensed version of a two-day software development workshop offered inside a major semiconductor company. Participants will be introduced to concepts and skills necessary to transform their software development practices and environment. The speakers will cover the pillars of modern software development: agile practices and methods, lean principles, user stories, scrum, and test-driven development. During the tutorial, all participants will participate in a hands-on scrum project.

Speakers:
Jan Acosta, **Karen Rosengren** - *IBM Corp., Round Rock, TX*

WORKSHOPS

W

Rm: 209AB

MULTIPROCESSOR SYSTEM-ON-CHIP (MPSOC): PROGRAMMABILITY, RUN-TIME SUPPORT AND HARDWARE PLATFORMS FOR HIGH PERFORMANCE APPLICATIONS AT DAC

Sunday, June 13 8:00am - 5:00pm

System-Level and Embedded

Lunch: 204AB
IEEE/ACM Member: $150 Non-Member: $195

Organizers: **Jürgen Becker** - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Diana Göhringer - *Fraunhofer IOSB, Ettlingen, Germany*
Andreas Herkersdorf - *Technische Univ. München, Munich, Germany*
Michael Hübner - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

For the next decade, Moore's Law is still going to bring higher transistor densities allowing billions of transistors to be integrated on a single chip. However, it became obvious that exploiting significant amounts of instruction-level parallelism with deeper pipelines and more aggressive wide-issue superscalar techniques, and using most of the transistor budget for large on-chip caches has come to a dead end. Especially, scaling performance with higher clock frequencies is getting more and more difficult because of heat dissipation problems and too high energy consumption. The latter is not only a technical problem for mobile systems, but is even going to become a severe problem for computing centers because high energy consumption leads to significant cost factors in the budget. Improving performance can only be achieved by exploiting parallelism on all system levels.

Multicore architectures offer a better performance/Watt ratio than single core architectures with similar performance. Combining multicore and coprocessor technology promise extreme computing power for highly CPU-time-consuming applications. Especially, FPGA-based accelerators not only offer the opportunity to speedup an application by implementing their compute-intensive kernels into hardware but also to adapt to the dynamical behavior of an application.

The purpose of the second edition of this very successful workshop is to evaluate strategies for future system design in MPSOC architectures. Both aspects, hardware design and tool-integration into existing development tools will be discussed. Especially, the novel trends in MPSOC combined with reconfigurable architectures are a topic in this workshop. The main emphasis is on architectures, design-flow, tool-development, applications and system design.

Speakers:
David Atienza Alonso - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*
Eshel Haritan - *Synopsys, Inc., San Jose, CA*
Hayden Kwok-Hay So - The *Univ of Hong, Hong Kong*
Tim Mattson - *Intel Corp., DuPont, WA*
Zhangxi Tan - *Univ. of California, Berkeley, CA*
Jürgen Teich - *Friedrich-Alexander-Univ. Erlangen-Nürnberg, Erlangen, Germany*
Lionel Torres - *LIRMM, Montpellier, France*

WORKSHOPS

W
Rm: 210AB

DAC WORKSHOP ON DIAGNOSTIC SERVICES IN NETWORK-ON-CHIPS (DSNoC) - 4TH EDITION

Sunday, June 13 8:30am - 5:30pm

Verification and Test

Lunch: 204AB
IEEE/ACM Member: $150 Non-Member: $195

Organizers: **Érika Cota** - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
Gert Jervan - *Tallinn Univ. of Technology, Tallinn, Estonia*
Thilo Pionteck - *Univ. zu Lübeck, Lübeck, Germany*

Network-on-Chips (NOCs) are settling as a new on-chip communication paradigm. Diagnostic services, such as test, debug, and on-line monitoring, are becoming an important factor in designing next-generation NOC-based systems.

The NOC infrastructure itself requires diagnostic services, and can also be used to support those for the entire system. Although significant research has been done in NOC design, there are many open and pressing issues regarding diagnostic services. The focus of this workshop is to explore them and their implications on system design. This is the fourth edition of DSNoC, after a sequence of successful events hosted by DATE (2007 and 2009) and DAC(2008). DSNoC 2010 is a one-day event with keynote address, one special session with invited papers, regular and poster presentations, and a panel session.

Speakers:
Paul Ampadu - *Univ. of Rochester, Rochester, NY*
Luca Carloni - *Columbia Univ., New York, NY*
Tim Cheng - *Univ. of California, Santa Barbara, CA*
Hannu Tenhunen - *Univ. of Turku, Turku, Finland*
Zeljko Zilic - *McGill Univ., Montreal, QB, Canada*

For more information please visit: www.dsnoc.org.

W
Rm: 206A

DAC WORKSHOP ON SYNERGIES BETWEEN DESIGN AUTOMATION AND SMART GRID

Sunday, June 13 8:00am - 6:00pm

General Interest

Lunch: 204AB
IEEE/ACM Member: $150 Non-Member: $195

Organizers: **Peter Feldmann** - *IBM Corp., Yorktown Hts., NY*
David Kung - *IBM Corp., Yorktown Hts., NY*
Jinjun Xiong - *IBM Corp., Yorktown Hts., NY*

The modernization of the world's electricity system to achieve the characteristics of a Smart Grid, namely, efficiency, reliability, resiliency, and security, is of highest priority in this energy constrained environment. These characteristics are also important metrics for hardware development where Design Automation (DA) has made significant progress in improving these metrics. The goal of this workshop is therefore to explore the potential of leveraging design automation techniques to benefit the development of Smart Grids.

This workshop intends to bring together world-class researchers and practitioners from both the power engineering and design automation communities to study the grand challenges facing this monumental transformation. It will provide a forum to share domain expertise, and to discuss the potential synergies between the two communities and how to join forces to solve these grand challenges. The Smart Grid initiative requires innovation in many areas but this workshop will focus on topics that have overlap with Design Automation - system management, simulation, modeling, optimization, fault detection, and security.

Speakers:
Shawn Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*
Joe Chow - *Rensselaer Polytechnic Institute, Troy, NY*
Ranjit Kumar - *InfSyn, LLC, Cupertino, CA*
Jan Rabaey - *Univ. of California, Berkeley, CA*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*
Li-C Wang - *Univ. of California, Santa Barbara, CA*
Brian Gaucher - *IBM Research, Yorktown Hts., NY*
Chee-Wooi - *Ten Michigan Technological University, Houghton, MI*
Hsiao-Dong Chiang - *Cornell University, Ithaca, NY*
Ingrid Verbauwhede - *Katholieke Universiteit Leuven Ingrid., Leuven-Heverlee, Belgium*
Jan M. Rabaey - *University of California, Berkeley, CA*
Joe Chow - *Rensselaer Polytechnic Institute,Troy, NY*
Li-C. Wang - *University of California, Santa Barbara, CA*
Marija Ilic - *Carnegie Mellon University, Pittsburgh, PA*
Peter Feldmann - *IBM Research Yorktown Hts., NY*
Ping Liu Hughes - *Research Laboratories, LLC, Malibu, CA*
Priscilla M. Lu - *Cathaya Funds, Redwoods, CA*
Ranjit Kumar - *InfSyn, LLC, Cupertino, CA*
Sachin Sapatnekar, *University of Minnesota, Minneapolis, MN*
Sani Nassif - *IBM Research, Austin, TX*
Shawn Blanton - *Carnegie Mellon University, Pittsburgh, PA*
Patrick Causgrove - *Bigwood Systems Inc, Ithaca, NY*

For more information please visit: http://www.datc.info/smartpower/.

WORKSHOPS

W
Rm: 303C

IWBDA: INTERNATIONAL WORKSHOP ON BIO-DESIGN AUTOMATION AT DAC

Monday, June 14 - Tuesday, June 15 8:00am - 6:00pm

General Interest

Lunch: 303D
IEEE/ACM Member $230 Non-Member $305

Organizers: **Douglas Densmore** - *Joint BioEnergy Institute, Emeryville, CA*
Marc Riedel - *Univ. of Minnesota, Minneapolis, MN*

The Second International Workshop on Bio-Design Automation (IWBDA) at DAC will bring together researchers from the synthetic biology, systems biology, and design automation communities. The focus is on concepts, methodologies and software tools for the computational analysis of biological systems and the synthesis of novel biological systems.

Still in its early stages, the field of synthetic biology has been driven by experimental expertise; much of its success has been attributable to the skill of the researchers in specific domains of biology. There has been a concerted effort to assemble repositories of standardized components. However, creating and integrating synthetic components remains an ad hoc process. The field has now reached a stage where it calls for computer-aided design tools. The electronic design automation (EDA) community has unique expertise to contribute to this endeavor. This workshop offers a forum for cross-disciplinary discussion, with the aim of seeding collaboration between the research communities.

Executive Committee:
General Chair - **Marc Riedel** - *University of Minnesota*
General Secretary - **Douglas Densmore** - *Joint BioEnergy Institute*
Program Committee Chair - **Ron Weiss** - *MIT*
Publication Chair - **Jean Peccoud** - *Virginia Tech, Blackburg, VA*
Industry Liaison Chair - **Andreas Kuehlmann** - *Cadence Research Labs*
Finance Chair - **David Thorsley** - *University of Washington*
DAC Liaison & Publicity Chair - **Soha Hassoun** - *Tufts University*

Keynote Speaker:
Roger Brent - *Fred Hutchinson Cancer Research Center, Seattle, WA*

Speakers:
J. Christopher Anderson - *UC Berkeley, Berkeley, CA*
Jacob Beal - *BBN Technologies, Cambridge, MA*
Deepak Chandran - *University of Washington, Seattle, WA*
Shawn Douglas - *Harvard Univ., Cambridge, MA*
Elisa Franco - *Caltech, Pasadena, CA*
Michal Galdzicki - *University of Washington, Seattle, WA*
Yiannis Kaznessis - *University of Minnesota, Minneapolis, MN*
KyungKim - *University of Washington, Seattle, WA*
Mario Andrea Marchisio - *ETH Zurich, Basel, Switzerland*
Richard Murray - *California Institute of Technology, Pasadena, CA*
Jean Pecoud - *Virginia Tech., Blackburg, VA*
Andrew Phillips - *Microsoft Research, Cambridge, United Kingdom*
Virgil Rhodius - *UCSF, San Francisco, CA*
Masoud Rostami - *Rice University, Houston, TX*
Pamela Silver - *Harvard Univ., Cambridge, MA*
Abiezer Tejeda - *Utah State University, Logan, UT*
Ehsan Ullah - *Tufts University, Medford, MA*
Mona Yousofshahi - *Tufts University, Medford, MA*

For more information please visit: http://www.biodesignautomation.org.

W
Rm: 206A

DAC WORKSHOP ON "MOBILE AND CLOUD COMPUTING"

Monday, June 14 8:30am - 5:15pm

General Interest

IEEE/ACM Member $150 Non-Member $195

Organizers: **Yung-Hsiang Lu** - *Purdue Univ., West Lafayette, IN*
Vijay Raghunathan - *Purdue Univ., West Lafayette, IN*

Mobile systems have become the primary computing platform for many users, in applications ranging from web surfing, communication, to multimedia. Meanwhile, cloud computing provides the opportunity to fundamentally change the way in which information is accessed, stored, and delivered. Cloud computing enables users to obtain high performance, large storage, and scalable service, without significant initial investment in hardware or software. This workshop explores how this emerging trend of cloud computing will impact the users of mobile systems. Speakers from industry and academia will share their views about the confluence of mobile and cloud computing, addressing various aspects of this topic. The workshop will also feature a panel discussing potential business opportunities for stakeholders in this area.

Speakers:
Cullen Bash - *Hewlett-Packard Labs, Palo Alto, CA*
Byung-Gon Chun - *Intel Corp., Berkeley, CA*
Chandra Narayanaswami - *IBM Corp., Hawthorne, NY*
Mahadev Satyanarayanan - *Carnegie Mellon Univ., Pittsburgh, PA*
Roy Want - *Intel Corp., Santa Clara, CA*
Ben Y. Zhao - *Univ. of California, Santa Barbara, CA*

For more information please visit:
https://engineering.purdue.edu/HELPS/DAC2010workshop.html.

WORKSHOPS

W
Rm: 204B

DAC WORKSHOP: MORE THAN CORE COMPETENCE...WHAT IT TAKES FOR YOUR CAREER TO SURVIVE, AND THRIVE! HOSTED BY WOMEN IN ELECTRONIC DESIGN (WWED)

Business

FREE

Monday, June 14 11:30am - 2:00pm

You do a good job. You take your work seriously. That should be all it takes for career success, right? If you think so, you need a wake up call!

Attend the DAC Workshop for Women in Electronic Design to hear Patty Azzarello explain why some get ahead, why some don't, and what you can do about it.

- Don't waste time and energy.
- Don't wait to be discovered.
- Don't let your career fall victim to someone else's priorities.

AGENDA HIGHLIGHTS:

Keynote Speaker: **Patty Azzarello** - *CEO, Palo Alto, CA of Azzarello Group*

Patty will show you how to take more control of your career, and get more success out of the effort you put into your job. She has 25 years of experience working in high tech and business. She became the youngest general manager at HP at the age of 33. She ran a $1B software business at the age of 35 and became a CEO for the first time at the age of 39.

The 2010 Workshop for Women in Electronic Design is supported by:

Panelist Presentations:

- Leadership with Authenticity"; Carol Hallett, VP Sales, Real Intent, Sunnyvale CA. In a business world primarily dominated by men, how can a woman bring her authentic self in a leadership position to be effective?
- Your Mentor: The Competitive Advantage For Your Career"; Gilda Garreton, Principal Engineer, SunLabs/Oracle, Redwood Shores, CA. Ever wonder about the value of having someone outside of your organization for independent advice? Mentoring is a leadership development tool; the key is how to use it.
- Money Talk: Pay, Compensation and Value"; Kathryn Kranen, CEO, Jasper Design Automation, Mountain View, CA. Diligence is not enough! Too many people are smart, busy and dedicated but the results, the value to their company is not there...or is not observable.

Additional details:

You're invited to join women and men in electronics, EDA and academia for this career building workshop. Lunch will be served to the first 150 people on a first come, first serve basis. The mid-day time allows workshop participants to attend DAC Free Monday Exhibits before and after, building a rewarding and full day at DAC.

Marie R. Pistilli Women in EDA Achievement Award

Women have made important contributions and strides in the EDA industry for over 20 years. In an effort to recognize those who have dedicated time towards these achievements, the DAC Executive Committee presents an annual award to honor an individual who has made significant contributions in helping women advance in the field of EDA technology. The Award presentation to the 2010 recipient will take place at WWED.

Special Thanks:

We would like to express our thanks to the DAC Executive Committee, ACM/SIGDA, DEDA, and the EDA Consortium for their support and leadership in making this event possible. Special thanks go to MP Associates, Inc. who donates the logistical and publication coordination for WWED.

COLOCATED EVENTS

C
Rm: 304A

IEEE INTERNATIONAL HIGH LEVEL DESIGN VALIDATION AND TEST WORKSHOP (HLDVT 2010)

Friday, June 11 - Saturday, June 12 8:00am - 6:00pm

Verification and Test

Organizers: **Prabhat Mishra** - *Univ. of Florida, Gainesville, FL*
Zeljko Zilic - *McGill Univ., Montreal, QB, Canada*

The 15th IEEE International High Level Design Validation and Test Workshop (HLDVT) advances research in validation and test methodologies for integrated circuits and systems. The workshop focuses on addressing the current bottlenecks in validation and test of complex and heterogeneous systems by both employing high-level specifications (such as register transfer level, behavioral and system-level models) and developing associated tools, techniques and methodologies to enable drastic reduction in overall design, validation and test effort. The workshop provides a forum for leaders in both industry and academia to advance the means for validating, debugging, synthesizing, and testing complex systems in a way that opens new avenues to overcome current validation and test challenges.

This year, HLDVT provides rich program including five regular sessions, five special sessions, one tutorial, one panel and one keynote speech. There are several areas of intense focus. First, there is one session on firmware validation and one session on HW-dependent software, to highlight the importance of embedded software. A session and a panel will be devoted to multi-clock systems and clock domain crossing verification, deployed in a variety of scenarios. One session will be devoted to transaction-level modeling, and another one will deal with high-level arithmetic circuit descriptions to obtain more from the circuits. Industry leaders in Electronic System Level (ESL) design will bring forward their perspectives on verification challenges at ESL, and a variety of papers will deal with formal verification advances, constraint solving, coverage and verification accelerators and emulators.

For more information please visit: http://www.hldvt.com/10/.

COLOCATED EVENTS

C
Rm: 207AB

IEEE/ACM 12TH INTERNATIONAL WORKSHOP ON SYSTEM LEVEL INTERCONNECT PREDICTION (SLIP)

Sunday, June 13 8:15am - 6:30pm

System-Level and Embedded

Organizers: **Deming Chen** - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Sherief Reda - *Brown Univ., Providence, RI*
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
Janet Wang - *Univ. of Arizona, Tucson, AZ*

The System-Level Interconnect Prediction (SLIP) Workshop focuses on modeling and prediction of the usable properties of optimized interconnect systems and their impact on system performance. Both theory and applications of interconnect prediction techniques are highlighted, with an emphasis on applications to architectural and micro-architectural exploration, physical design, interconnect technology planning and communication networks. In addition to the presentation of state-of-the-art papers in these fields, invited talks and tutorials by leading researchers will aim to encourage dialogue between the architecture, physical design, and interconnect technology communities.

SLIP 2010 will feature special sessions on System-Level Interconnect Prediction for Emerging Technologies, with emphasis on 1) the implications of many-core architectures on system-level interconnect design, 2) the utilization of emerging technologies (e.g., 3-D integration and photonics networks) in system-level interconnect planning and synthesis, 3) high-speed PCB routing and chip-package co-design, and 4) future research directions for SLIP.

Representative technical topics include:

- Interconnect prediction at various IC design stages
- Interconnect design challenges and system-level NoC design
- Design and analysis of power and clock networks
- Interconnect architecture of structural designs and FPGAs
- Interconnect fabrics of many-core architectures
- Design-for-manufacturing (DFM) techniques for interconnects
- High speed PCB interconnect design
- Design and analysis of chip-package interfaces
- Interconnect topologies of multiprocessor systems
- Interconnect design using through-silicon vias (TSV) in 3-D ICs
- Emerging interconnect technologies, e.g., RF interconnects, photonic networks, carbon-based interconnects, etc.

For more information please visit: http://www.sliponline.org.

C
Rm: 208AB

SYSTEM AND SOC DEBUG INTEGRATION AND APPLICATIONS

Sunday, June 13 9:00am - 6:00pm

System-Level and Embedded

Organizers: **Adam Morawiec** - *ECSI, Gieres, France*
Neal Stollon - *HDL Dynamics, Dallas, TX*

Debug in SOC and electronic systems is a major and ongoing issue for all complex products. Most SOC level ICs and an increasing number of systems include complex instrumentation for debug and related purposes. Different types of debug and instrumentation embedded in a system are varied and often depend both on end application and analysis requirements. Having embedded instrumentation in a design provides a major advantage and compliment to other analysis techniques as it allows real time visibility into the actual system, rather than just models. It is a capability and analysis flow that continues to evolve and improve. Among the capabilities needed in instrumentation and debug flows are tools to support both the automation and integration of instrumentation capability with other analysis methods. Much of the sophisticated infrastructure and analysis tools for design automation may be applied to debug tasks. There are major potential benefits to both the end users and EDA community in reuse of design automation tools, both commercial and open-source, for debug related applications in improving the verification and analysis of SOCs and improving time to market and quality of silicon products.

The types of instrumentation and debug requirements can vary significantly for different types of systems. Software and processor-centric systems have different debug requirements from logic based systems (such as FPGA). High reliability applications such as medical and aerospace have different requirements from entertainment and consumer products, which differ in turn from industrial systems such as networks, and as such require each different investments, both in hardware and development time.

Recent years have seen significant of activity into standardization of the interfaces, features, and methodologies related to SOC and systems debug. These include development work going into the standardization of the debug and software interfaces for multicore and distributed processing systems, which challenge in scaling instrumentation and debug and software development tools to support chips with many cores and the related software and analysis methods required to support them.

This workshop, based on the successful workshops organized by ECSI in 2007, 2008, and 2009, also provides an overview and update into several standards efforts related to SOC and system debug with representation from IEEE working groups including Nexus Forum, IJTAG (IEEE P1687), IEEE 1149.7 as well as working groups within the OCP-IP, Multicore Association, and Eclipse consortiums. It presents the features and commonalities of a vast set of requirements expressed by the system and SOC companies with regard to debug methods and tools will also present and contrast existing commercial debug tools and research into for different applications in these areas.

For more information, please visit: http://www.ecsi.org/dac-system-and-soc-debug.

C
Rm: 207C

DESIGN FOR MANUFACTURABILITY COALITION WORKSHOP - "A NEW ERA FOR DFM"

Sunday, June 13 1:00 - 4:00pm

DFM and the Manufacturing Interface

Organizers: **Bill Bayer** - *Si2, Austin, TX*
Jake Buurma - *Si2, Austin, TX*

The workshop will educate the audience on a high level DFM verification and optimization language called OpenDFM. OpenDFM rules bridge the gap between a layout style that allows only a few, very restricted layout patterns and a style that allows purely arbitrary layouts. OpenDFM functions transform database shapes, regardless of their origin and design style, into the on-silicon target shapes that design and manufacturing both agree are the reference shapes for silicon based measurements and extraction. OpenDFM increases the level of pattern uniformity in the layout and it polishes the rough spots in the layout when it finds layout patterns that are known to be problematic. OpenDFM modifies the design to physically optimize and measurably affect electrical performance to enhance Process Limited Yield (PLY) and/or Circuit Limited Yield (CLY) during the design process and not at post tapeout.

For more information please visit: http://www.si2.org/?page=1146.

COLOCATED EVENTS

C

NORTH AMERICAN SYSTEMC USERS GROUP (NASCUG 13 MEETING)

Sunday, June 13 3:30 - 7:30pm

Rm: Hilton Anaheim

System-Level and Embedded

Organizers: **Jill Jacobs** - *OSCI, San Jose, CA*

The North American SystemC User's Group (NASCUG) invites you to a special event featuring the latest advancements in sustainable and flexible solutions for ESL design. Technical presentations on architectural modeling, transaction-level modeling and analog/mixed-signal design using SystemC™ will be featured. Interact with colleagues and industry experts, and find out first-hand how system-level design with System has become a nuts-and-bolts part of the designer's toolbox.

Preliminary Agenda

3:30 - 4:00pm: Registration

4:00 - 4:10pm: Welcome and Agenda

4:10 - 4:30pm: OSCI and Technical WG Update

4:30 - 6:45pm: Technical Presentations

6:45 - 7:30pm: Networking Reception

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C

Rm: 207D

8TH IEEE SYMPOSIUM ON APPLICATION SPECIFIC PROCESSORS (SASP 2010)

Sunday, June 13 - Monday, June 14 8:00am - 6:00pm

System-Level and Embedded

Organizers: **Philip Brisk** - *Univ. of California, Riverside, CA*
Tulika Mitra - *National Univ. of Singapore, Singapore*
Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

The market for embedded processors is driven primarily by two factors: cost and volume. This has forced a reevaluation of the best way to satisfy users' needs for high performance and low energy consumption without drastically increasing the complexity of the design process. Domain-specific embedded processors, in markets such as network processing, automotive, and others, have splintered a pre-existing market for general-purpose, low-cost, low-energy processors. Reprogrammable and reconfigurable embedded processors, in contrast, offer a single, fixed-silicon device that could amortize manufacturing costs for low-to-medium volume market segments. SASP explores (micro)architectural design approaches, trade-offs and compiler technologies, for both domain-specific and customizable embedded processors. The symposium is a forum wherein challenges and solutions will be explored, discussed and compared.

For more information please visit: www.sasp-conference.org.

C

Rm: 205AB

INTERNATIONAL SYMPOSIUM ON HARDWARE-ORIENTED SECURITY AND TRUST (HOST)

Sunday, June 13 - Monday, June 14 7:30am - 6:00pm

General Interest

Organizers: **Ken Mai** - *Carnegie Mellon Univ., Pittsburgh, PA*
Jim Plusquellic - *Univ. of New Mexico, Albuquerque, NM*

The emergence of a globalized, horizontal semiconductor business model raises a set of concerns involving the security and trust of the information systems on which modern society is increasingly reliant for mission-critical functionality. Hardware-oriented security and trust (HOST) issues span a broad range including threats related to the malicious insertion of Trojan circuits designed, e.g., to act as a 'kill switch' to disable a chip, to integrated circuit (IC) piracy, and to attacks designed to extract encryption keys and IP from a chip. HOST covers security and trust issues in all types of electronic devices and systems such as ASICs, COTS, FPGAs, microprocessors/DSPs, and embedded systems. The mission of HOST is to provide a forum for the presentation and discussion of research that is of critical significance to the security of, and trust in, modern society's microelectronic-supported infrastructures.

The IEEE International Symposium on Hardware-Oriented Security and Trust (HOST 2010) provides an open forum for discussions on all issues related to hardware security and trust. Papers and presentations that address any of the following "hot topics" are of high interest to the symposium. Papers addressing HOST issues outside of these areas will be considered equally relevant in the review process.

For more information please visit: www.engr.uconn.edu/HOST.

COLOCATED EVENTS

C
Rm: 207AB

4TH IEEE INTERNATIONAL WORKSHOP ON DESIGN FOR MANUFACTURABILITY & YIELD (DFM&Y)

Monday, June 14 8:30am - 5:30pm

DFM and the Manufacturing Interface

Organizers: **Rob Aitken** - *ARM Ltd., San Jose, CA*
Puneet Gupta - *Univ. of California, Los Angeles, CA*,

Increased manufacturing challenges in today's nanometer technologies require up to date solutions for yield optimization. Designing an SOC for manufacturability and yield aims at improving the manufacturing process and consequently its yield by enhancing communications across the design – manufacturing interface. A wide range of Design-for-Manufacturability (DFM) and Design-for-Yield (DFY) methodologies and tools are in use today. Some of these are applied during the back-end design stages, including mask design, while others involve post design activities, from lithography through wafer sort, packaging, final test and failure analysis. DFM can dramatically impact the business performance of chip manufacturers. It can also significantly affect age-old chip design flows. Using a DFM solution is an investment and thus choosing the most cost effective one(s) requires trade-off analysis. The workshop analyzes the key trends and challenges in DFM&Y, and provides an opportunity to discuss a range of DFM and DFY solutions for SOC designs now and in the future.

Please visit: http://vlsicad.ucsd.edu/DFMY for more details.

C
Rm: 208AB

CHOOSING ADVANCED VERIFICATION METHODS: SO MANY POSSIBILITIES, SO LITTLE TIME

Monday, June 14 9:00am - 5:00pm

Verification and Test

Organizer: **Adam Morawiec** - *ECSI, Gieres, France*

Significant improvements in verification effectiveness have been achieved through recent technology developments in the areas of formal verification, constrained-random simulation, high-level design/verification, and verification planning [or emulation???]. In order to plan for methodology upgrades, designers and verification engineers need to understand what are the measurable results of the integration of these methods into real-world design flows.

The workshop will present a survey of recent verification solution advances and will bring insight into the effects these technologies are having on leading edge design projects. Measurable impact on quality, time-to-market, schedule, efficiency, and actual ROI will be analyzed. Participants will be able to hear from real customers about their verification problems and their experiences in the deployment of these technologies.

For more information, please visit: http://www.ecsi.org/dac-verification-methods.

C
Rm: 207C

ADVANCES IN PROCESS DESIGN KITS WORKSHOP

Monday, June 14 1:00 - 4:00pm

General Interest

Organizers: **Sumit DasGupta** - *Si2, Austin, TX*
Nick English - *Si2, Austin, TX*

Process Design Kits (PDKs) are the fundamental building blocks for all electronic design. Adopting a set of standards to specify PDK content and interfaces will offer many advantages. Foundries will be able to offer fewer, more robust kits thus reducing their costs and increase their ability to communicate the essential functionality, performance, predictability, and reusability of their OpenPDKs to the rest of the industry. EDA companies will be able to write tools to standard data definitions and interfaces to enable a higher level of interoperability and consistent usage across tools and flows. For end-users, the resultant reduction in barriers to migrating designs and reusing IP will ease their design challenges thus accelerating their path to working silicon. This workshop will introduce all of the aspects of PDKs and the presenters will describe the state-of-the-art and make recommendations for future work in the following areas. Interoperable Schematic Symbols, Design Parameter Specification, Callback Specifications, Pcells, SPICE Sockets, Technology File enhancements, and Process Retargeting and Verification. The workshop is aimed at providers and consumers of Process Design Kits from across the industry.

For more information, please visit: http://www.si2.org/?page=1145.

Speakers: **Steve Schulz** - *Si2, Austin, TX*
James Masters - *Intel Corp., Folsom, CA*
Jose A. Del Cano - *Intel Corp., Santa Clara, CA*
Tom Quan - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*
Pankaj Mayor - *Cadence Design Systems, Inc., San Jose, CA*
John Stabenow - *Cadence Design Systems, Inc., San Jose, CA*
Linda Fosler - *Mentor Graphics Corp., San Jose, CA*
Duncan McDonald - *SpringSoft, Inc., San Jose, CA*

C
Rm: 204AB

ACM STUDENT RESEARCH COMPETITION

Tuesday, June 15 - Wednesday, June 16 2:00 - 4:00pm

General Interest

Organizers: **Iris Bahar** - *Brown Univ., Providence, RI*
Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

Sponsored by Microsoft Research, the ACM Student Research Competition is an internationally recognized venue enabling undergraduate and graduate students who are ACM members to:

- Experience the research world - for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees
- Rub shoulders with academic and industry luminaries
- Understand the practical applications of their research
- Perfect their communication skills
- Receive prizes and gain recognition from ACM and the greater computing community

The ACM Special Interest Group on Design Automation is organizing such an event in conjunction with the Design Automation Conference. Authors of accepted submissions will get travel grants from ACM/Microsoft to attend the event at DAC. The event consists of several rounds, as described at http://www.acm.org/src/participate.html and http://www.acm.org/src/about.html culminating with awards given in the graduate and undergraduate student category, and the ACM Grand Finals Competition

COLOCATED EVENTS

C

Rm: 205AB

NASA/ESA CONFERENCE ON ADAPTIVE HARDWARE AND SYSTEMS (AHS-2010)

Tuesday, June 15 - Friday, June 18

General Interest

Organizers: **Tughrul Arslan** - *Univ. of Edinburgh, Edinburgh, Scotland, United Kingdom*
Khaled Benkrid - *Univ. of Edinburgh, Edinburgh, Scotland, United Kingdom*
David Merodio Codinachs - *ESA, Noordwijk, The Netherlands*
Ahmet Erdogan - *Univ. of Edinburgh, Edinburgh, Scotland, United Kingdom*
Tetsuya Higuchi - *AIST, Tokyo, Japan*
Didier Keymeulen - *NASA's Jet Propulsion Lab, Pasadena, CA*
Umeshkumar Patel - *Goddard Space Flight Center, Greenbelt, Maryland*
Matin Suess - *ESA, Noordwijk, The Netherlands*

Tuesday, June 15	10:00am - 6:00pm
Wednesday, June 16	9:00am - 6:00pm
Thursday, June 17	9:00am - 6:00pm
Friday, June 18	9:00am - 5:00pm

The purpose of the NASA/ESA Adaptive Hardware and Systems (AHS) conference is to bring together leading researchers from the adaptive hardware and systems community to exchange experiences and share new ideas in the field.

Adaptation reflects the capability of a system to maintain or improve its performance in the context of internal or external changes, such as uncertainties and variations during fabrication, faults and degradations, modifications in the operational environment, incidental or intentional interference, different users and preferences, modifications of standards and requirements, trade-offs between performance and resources.

Adaptation at hardware levels increases the system capabilities beyond what is possible with software-only solutions, and a large number of adaptation features employing both analog and digital adjustments are becoming increasingly present in the most elementary system components. Algorithms, techniques, and their implementation in hardware are developed over a diverse variety of applications, such as adaptive communications (adapting to changing environment and interferences), reconfigurable systems on a chip and portable wireless devices (adapting to power limitations) or survivable spacecraft (adapting to extreme environments and mission unknowns). This meeting will provide a forum for discussion on the generic techniques of adaptive hardware and systems, with a focus on communications and space applications, with view to its expansion and exploitation in other applications such as consumer, medical, defense and security.

KEYNOTE SPEAKERS: **Barry Goldstein** - *Manager of Autonomous Systems Division, Jet Propulsion Laboratory Gianfranco Visentin - Head of Automation and Robotics Section, ESA/ESTEC*

For more information: http://www.see.ed.ac.uk/~ahs2010/.

C

Rm: 204C

IEEE/ACM INTERNATIONAL SYMPOSIUM ON NANOSCALE ARCHITECTURES (NANOARCH'10)

Thursday, June 17 - Friday, June 18 8:00am - 6:00pm

General Interest

Organizers: **Shamik Das** - *The MITRE Corp., McLean, VA*

NANOARCH is the annual forum for the presentation and discussion of novel nanoelectronic circuit and system architectures. The NANOARCH symposium seeks papers on innovative ideas for solutions to the principal challenge facing integrated electronics in the 21st century–how to design, fabricate, and test circuits and systems that will have to rely upon devices beyond conventional CMOS. In particular, such systems will (1) contain anywhere from a hundred to a trillion unconventional nanodevices with unique functionalities, (2) need to cope with unavoidably high levels of defects and faults, and (3) require rethinking of the methodologies involved, from the construction of basic logic gates / functional units to the compilation and mapping of high-level programs onto novel nanoscale computational fabrics.

This 6th symposium seeks to build on the successes of the previous five iterations of NANOARCH (2005-2009). The symposium's topics of interest include (but are not limited to) the following:

- Ideas for novel nanoelectronic circuits or system architectures that resolve key issues anticipated in the design, fabrication, and operation of nanoelectronic systems
- Performance simulations of nanoscale architectures, macro blocks, or key nanocircuits
- Novel implementations of microarchitecture concepts using nanoscale building blocks
- Computational paradigms and programming models for nanoscale architectures
- Methodologies for incorporating defect and fault tolerance
- Validation frameworks for ensuring correct functionality in defective nanoscale fabrics
- Computer aided design tools and methodologies for nanoelectronic architectures
- Experimental assessment and/or validation of nanoscale architectural concepts

For more information, please visit: http://www.nanoarch.org/10/index.html.

C

19TH INTERNATIONAL WORKSHOP ON LOGIC AND SYNTHESIS (IWLS)

Friday, June 18 - Sunday, June 20

Univ. of California, Irvine

Synthesis and FPGA

Organizers: **Valeria Bertacco** - *Univ. of Michigan, Ann Arbor, MI*
Philip Brisk - *Univ. of California, Riverside, CA*
Igor Markov - *Univ. of Michigan, Ann Arbor, MI*

The International Workshop on Logic and Synthesis is dedicated to research in synthesis, optimization, and verification of integrated circuits. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop accepts complete papers as well as abstracts highlighting important new problems in the early stages of development. The emphasis is on novelty and intellectual rigor.

For more information, please visit: http://www.iwls.org/.

ADJUNCT EVENTS

CEDA: "BEYOND VON NEUMANN COMPUTING"

AE Rm: 303AB

Tuesday, June 15 12:00 - 2:00pm

General Interest

The "von Neumann architecture" for computers, invented mostly by Turing but popularized by the more famous von Neumann, has completely dominated computing for more than 65 years. It is a masterpiece of simplicity: readily implemented in hardware, easily understood by software developers, and amenable to compilation from a wide variety of programming languages. Unfortunately, it achieves its simplicity from the fundamental, non-physical assumption that reading from a memory location takes negligible, constant time independent of the size of the memory. Decades of innovation in computer architecture and compiler design for uniprocessors has masked some of the von Neumann computer's intrinsic latency. The power requirements for this disguise have become prohibitive, though, which has ended the long, exponential rise in uniprocessor clock frequency. Multicore processors, the semiconductor industry's response, have the virtue that they can clearly be built, but no one knows how to program them! Further, they make the same negligible-latency assumptions as uniprocessors, but disguising that latency is now quadratically more difficult.

This talk will show that highly useful yet non-physical oversimplifications such as the von Neumann architecture have numerous historical precedents from which we can learn. These examples suggest that a more physically aware, non-von Neumann machine could offer higher-performance and far more power-efficient computation. Next, we offer some thoughts on what such a machine might look like - hint: it is not an array of microprocessors! - and how one might program it. It is only by simultaneously approaching architecture, hardware, and software, seeing them as aspects of a cohesive whole as von Neumann and Turing both did, that we maximize our chances of going beyond von Neumann computing.

Lunch will be served to the first 150 attendees. There will be additional seating available.

Speaker:
Steve Teig - *Tabula, Inc., Santa Clara, CA*

13TH ANNUAL SIGDA PH.D. FORUM / MEMBER MEETING

AE Rm: 204A

Wednesday, June 16 6:00 - 7:30pm

General Interest

Organizer: **Alex Jones** - *Univ. of Pittsburgh, Pittsburgh, PA*

SIGDA invites you to attend our 13th annual Ph.D. Forum and Member Meeting at DAC 2010. SIGDA members are invited, as are all members of the EDA Community. We will begin with an overview of SIGDA programs including newly created programs, followed by the presentation of this year's ACM/SIGDA Awards. However, the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives students feedback on their research, and gives the EDA community a preview of work in progress. Light refreshments will be served.

SIGDA/DAC UNIVERSITY BOOTH

Tuesday, June 15 - Wednesday, June 16 10:00am - 5:00pm

This year marks the 23rd University Booth at the Design Automation Conference. The booth is an opportunity for university researchers to display their results and to interact with participants at DAC. The demonstrations include new EDA tools, EDA tool applications, design projects, and instructional materials.

The University Booth has a new and improved format this year:

i) The University Booth is relocating to a premium location off the technical sessions for improved visibility.

ii) The project submission is in a video presentation format, with live demonstrations performed at the booth.

The ISSCC/DAC Design Contest winners are also invited to give demonstrations presenting their work at the University Booth. The schedule of presentations is published at the conference and is also available on the SIGDA website at http://www.sigda.org/ubooth.html. The organizers thank the Design Automation Conference for its continued support of this project.

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47 DESIGN AUTOMATION CONFERENCE

EXHIBITION HIGHLIGHTS

The 47th DAC exhibition is located in Halls B and C of the Anaheim Convention Center.

Visit the DAC exhibition for an in-depth view of new products and services from nearly 200 vendors spanning all aspects of the electronic design process, including EDA tools, IP cores, embedded system and system-level tools, as well as silicon foundry and design services.

DAC PAVILION

The popular DAC Pavilion is located in Hall C in Booth 694. The DAC Pavilion will feature 16 presentations on business and technical issues.

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EXHIBITOR FORUM

The Exhibitor Forum provides a theater on the exhibit floor where exhibitors present focused, practical technical content to attendees. The presentations are selected by an all-user Exhibitor Forum Committee chaired by Magdy Abadir of Freescale Semiconductor, Inc. Each session is devoted entirely to a specific domain (e.g., verification or system-level design) and consists of presentations from three companies.

The Exhibitor Forum is in Hall B in Booth 1562. Topics include: System-Level Design/Embedded Software, Physical Design and Sign-Off, Verification, Power Management/Signal Integrity, Analog/Mixed-Signal and RF, Design for Manufacturability, Intellectual Property Cores, Design for Test and Manufacturing Test, Package Design, and Silicon Validation and Debug.

EXHIBITOR FORUM

EXHIBIT-ONLY PASS

Register for an exhibit-only pass and receive admission to all days of the exhibition, all Keynotes, all DAC Pavilion and Exhibitor Forum sessions, the IC Design Central Partner Pavilion, plus the Tuesday night party.

THE IC DESIGN CENTRAL PARTNER PAVILION—PUTTING MORE DESIGN INTO DAC

The IC Design Central Partner Pavilion, located in Hall B, stage #1710, brings together vendors supplying products and services that address many of the critical design functions necessary to produce working silicon on time and on budget. Companies from all areas of the design and product development process—EDA, Foundry, IP, Design Services, Assembly/Package, Test, and System Interconnect—must cooperate to offer integrated front-to-back solutions that ensure first-time-successful silicon and predictable time-to-market. Visit the ICDC Partner Pavilion and find design flows and solutions needed to create today's challenging designs.

The ICDC Partner Pavilion is a combination of exhibit booths and 30-minute presentations by each participating vendor. The combination of product displays in the exhibits and technical product presentations in the ICDC Theater offers attendees an in-depth look into flows and methodologies from vendors featuring a variety of products and services for the entire design ecosystem.

iCDC

Current participating ICDC exhibitors include:

Altair Engineering
Amiq Consulting S.R.L.
ASIC Analytic, LLC
Avant Technology Inc.
BEEcube, Inc.
Cambridge Analog Technologies
CoFluent Design
Chip Vision
CISC Semiconductor Design & Consulting
Enterpoint Ltd.
ExpertIO, Inc.
Gary Stringham & Associates, LLC
IBM Corp.
iNoCs
Progate Group Corp.
R3 Logic Inc.
TSSI - Test Systems Strategies, Inc.
X-FAB Semiconductor Foundries
Zocalo Tech, Inc.

EXHIBITION HOURS

Monday, June 14 - Wednesday, June 16
9:00am - 6:00pm

PAVILION PANELS
EXHIBIT HALL C, BOOTH #694

PP

GARY SMITH ON EDA: TRENDS AND WHAT'S HOT AT DAC

Monday, June 14 9:15 - 10:15am

General Interest

Chair: **Gary Smith** - *Gary Smith EDA, Santa Clara, CA*
Organizer: **Robert Gardner** - *EDA Consortium, San Jose, CA*

Speaker:
Gary Smith - *Gary Smith EDA, Santa Clara, CA*

Gary Smith of Gary Smith EDA reviews EDA's hottest technology trends. How will the dramatic changes in EDA, the semiconductor market and the design community affect you? What are the hot 'must sees' at this year's conference? Find out here!

PP

THE MULTIPLIER EFFECT: DEVELOPING MULTICORE, MULTI-OS APPLICATIONS

Monday, June 14 10:30 - 11:15am

System-Level and Embedded

Chair: **Paul Dempsey** - *EDA Tech Forum, Falls Church, VA*
Organizer: **Laura Parker** - *Mentor Graphics Corp., Wilsonville, OR*

Speakers:
Daniel Forsgren - *Enea, Kista, Sweden*
Alan Gatherer - *Huawei Technologies Co., Ltd., Dallas, TX*
Simon Milner - *Marvell Semiconductor, Inc., Santa Clara, CA*

A growing number of designers are creating architectures that run multiple operating systems on multiple cores to optimize system performance, efficiently manage power and meet portability requirements. How are design teams today adopting a multicore, multi-OS approach? Panelists will look at the benefits and challenges and discuss development environments needed for effective application creation when using multiple, heterogeneous operating systems.

PP

CAREER OUTLOOK: JOB MARKET 2010

Monday, June 14 11:30am - 12:15pm

General Interest

Chair: **Rick Nelson** - *Canon Communications, Lexington, MA*
Organizer: **Tiffany Sparks** - *GLOBALFOUNDRIES, Milpitas, CA*

Speakers:
Mark Gilbert - *EDA Careers, Miami, FL*
Rob Dumas - *DICE GmbH & Co. KG, Bellevue, WA*

The economic downturn wreaked havoc on the job market - but what's the outlook moving forward? What geographies and market segments are hot? What skills are in demand? When you find a job, with there be changes in salary and compensation? Experts discuss the outlook for the industry's job market and offer advice for safe-guarding your career moving forward.

PP

OUTSOURCING DOESN'T MEAN OFF-SHORING— WHAT IS IT? AND, WHY DO IT?

Monday, June 14 1:30 - 2:15pm

Business

Chair: **Ron Wilson** - *EDN Magazine, San Jose, CA*
Organizer: **Susan Cain** - *Cain Communications, Inc., Newberg, OR*

Speakers:
Hugh Durdan - *eSilicon Corp., Sunnyvale, CA*
Lee Smith - *Amkor Technology, Chandler, AZ*
James VanAntwerp - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*

The reach of outsourcing continues to expand from packaging and test to EDA and wafer manufacturing, to IP and front-end design services. What's next...an outsourced CEO? Where does it stop? Fabless companies and System OEMs have access to many more resources within the supply chain. What's the right balance? Panelists will discuss make/buy decisions, global operations, and economic trends influencing the semiconductor industry.

PAVILION PANELS
EXHIBIT HALL C, BOOTH #694

PP

EDA HERITAGE - MEET VERILOG INVENTOR DR. MOORBY AND FORMAL VERIFICATION PIONEER PROF. BRYANT

Monday, June 14 2:30 - 3:15pm

General Interest

Chair: **Bryon Moyer** - *IC Design and Verification Journal, Portland, OR*
Organizer: **Shishpal Rawat** - *Intel Corp., Folsom, CA*

Speakers:
Randal E. Bryant - *Carnegie Mellon Univ., Pittsburgh, PA*
Phil Moorby - *Sigmatix, Inc., Chelmsford, MA*

Phil Kaufman award winners Randal Bryant (2009) and Phil Moorby (2005) discuss the impact of commercializing their inventions. Bryant's work to formally verify digital hardware revolutionized the field, enabling reasoning about large-scale circuit designs for the first time. Moorby invented Verilog, raising the level of abstraction for electronic designs. Learn what challenges and opportunities they see for the electronics industry.

PP

A CONVERSATION WITH THE 2010 MARIE PISTILLI AWARD WINNER

Monday, June 14 3:30 - 4:15pm

General Interest

Chair: **Peggy Aycinena** - *EDA Confidential & EDAMarket, San Mateo, CA*
Organizer: **Sabina Burns** - *Virage Logic Corp., Fremont, CA*

Join the 2010 Marie R. Pistilli Award Winner in a one-on-one conversation with EDA Confidential's Peggy Aycinena. As always, the conversation promises to be lively and wide-ranging, with ample opportunity for audience participation in a discussion that spans both gender and generational issues.

PP

HOGAN'S HEROES: WHAT DESIGN AND LITHOGRAPHY NIGHTMARES WILL 22nm BRING?

Tuesday, June 15 10:30 - 11:30am

General Interest

Chair: **Jim Hogan** - *Vista Ventures LLC, Campbell, CA*
Organizer: **Jan Willis** - *Calibra Consulting, Aylesbury, United Kingdom*

Speakers:
Aki Fujimura - *D2S, Inc., San Jose, CA*
Xin Wu - *Xilinx, Inc., San Jose, CA*
Aaron Thean - *Qualcomm, Inc., Austin, TX*

A leading processor company said they lose sleep over low-power, not lithography - will their perspective change at 22nm? Will the limits of lithography impose new rules for designers? Which innovations and rules are likely to prevail and what will be their impacet on cost, performance, power and time-to-market?

PP

EVERYONE LOVES A TEARDOWN

Tuesday, June 15 1:30 - 2:15pm

General Interest

Organizer: **Andrea Kroll** - *Huawei Technologies Co., Ltd., Santa Clara, CA*

Speaker:
Mike Thompson - *Virage Logic Corp., Fremont, CA*

Ever wonder what's inside of that latest laptop? We're going to show you. In this session, we share details about the inside of the chips inside a laptop - challenges faced, innovative solutions created, IPs used and unique software embedded. Some of what's in there is surprising like the eight 32-bit ARC processors and Virage Logic memory cells. Let's look inside!

PAVILION PANELS
EXHIBIT HALL C, BOOTH #694

PP

IS THE FPGA TOOL OPPORTUNITY AN OASIS OR A MIRAGE?

Tuesday, June 15 2:30 - 3:15pm

Synthesis and FPGA

Chair: **Kevin Morris** - *FPGA Journal/Techfocus Media, Portland, OR*
Organizer: **Mike Santarini** - *Xilinx, Inc., San Jose, CA*

Speakers:
Jacques Benkoski - *US Venture Partners/Synfora, Inc., Menlo Park, CA*
Simon Bloch - *Mentor Graphics Corp., Wilsonville, OR*
Andrew Dauman - *Synopsys, Inc., Sunnyvale, CA*

EDA companies have traditionally shied away from the FPGA community. As ASIC starts continue to fall and with IPO options dwindling, should the EDA industry direct its attention to better serve the FPGA user base - now 100,000 and growing? What are the opportunities for third-party tool providers? FPGA users be heard, tell the panelists what you want in your design tools.

PP

28nm AND BELOW: SOC DESIGN ECOSYSTEM AT A CROSSROAD

Tuesday, June 15 3:30 - 4:15pm

General Interest

Chair: **Ed Sperling** - *Low-Power Design, San Francisco, CA*
Organizer: **Mike Sottak** - *Wired Island Ltd., Providenciales, Turks and Caicos Islands*

Speakers:
Mojy Chian - *GLOBALFOUNDRIES, Sunnyvale, CA*
Mark Ireland - *IBM Corp., Burlington, VT*
Naveed Sherwani - *Open-Silicon, Inc., Milpitas, CA*

28nm presents an inflection point. Pre-packaged EDA, IP and foundry solutions aren't enough. Few semiconductor companies appear equipped to reap the full benefits of the node in keeping with Moore's Law. If foundries are turning to a virtual IDM model or even an ASIC-like approach, how will business models evolve to address time to market and development cost constraints?

PP

HOT AND SPICEY: USERS REVIEW DIFFERENT FLAVORS OF SPICE AND FAST SPICE

Tuesday, June 15 4:30 - 5:15pm

Analog/Mixed-Signal/RF Design

Chair: **Daniel Payne** - *Marketing EDA, Tualatin, OR*
Organizer: **Daniel Payne** - *Marketing EDA, Tualatin, OR*

Speakers:
Aaron Barker - *Oracle, Broomfield, CO*
Pierluigi Daglio - *STMicroelectronics, Agrate, Italy*
Jin-Qin Lu - *Atheros Communications, Inc., Santa Clara, CA*

Are you one of the 20,000 analog and mixed-signal designers stuck waiting for your SPICE simulation run to complete today? Inexpensive multicore hardware, multithreaded software, and new algorithms promise to deliver SPICE accuracy 10- to 100-times faster than earlier methods. The panelists have evaluated the new generation of fast SPICE products and will discuss the tradeoffs of each approach from a users' perspective.

PP

LUCIO'S LITMUS TEST: IS YOUR START-UP READY FOR THE 21ST CENTURY?

Wednesday, June 16 9:15 - 10:15am

Business

Chair: **Lucio Lanza** - *Lanza techVentures, Palo Alto, CA*
Organizer: **Dave Millman** - *Ciranova, Inc., Santa Clara, CA*

Speakers:
Philippe Faes - *Sigasi bvba, Ghent, Belgium*
Evan Lavelle - *Maia EDA Ltd., Cambridge, United Kingdom*
Yunshan Zhu - *NextOp Software, Inc., Santa Clara, CA*

Everything about starting an EDA business today is very different - from securing financing to assembling teams to building channels all the way to a successful exit strategy. Serial entrepreneur Lucio Lanza will listen to three EDA start-up pitches and share his opinions on how they can succeed in today's environment. Get valuable tips whether you're in a budding start-up or established company.

PAVILION PANELS
EXHIBIT HALL C, BOOTH #694

PP

IP COMMERCIALIZATION: BEYOND THE CODE
Wednesday, June 16 10:30 - 11:15am

Business

Chair: **Adam Traidman** - *Cadence Design Systems, Inc., San Jose, CA*
Organizer: **Brenda Westcott** - *Virage Logic Corp., Fremont, CA*

Speakers:
Marc Greenberg - *Denali Software, Inc., Austin, TX*
Jonathan T. Kaplan - *Law Office of Jonathan T. Kaplan, Vancouver, WA*
Mike Thompson - *Virage Logic Corp., Fremont, CA*

Creating valuable IP is difficult but commercializing it is much more challenging. What levels of simulation, silicon validation and legal protection are required to enable a successful production release? Hear IP experts discuss the challenges they face in terms of quality, silicon proven process, integration, support and licensing terms.

PP

HIGH-SCHOOL PANEL: YOU DON'T KNOW JACK!
Wednesday, June 16 2:30 - 3:15pm

General Interest

Chair: **Kathryn Kranen** - *Jasper Design Automation, Inc., Mountain View, CA*
Organizer: **Yatin Trivedi** - *Synopsys, Inc., Mountain View, CA*

High School students tell us how they use the latest tech gadgets, and what they expect to be using in 2 to 3 years. They are the early predictors of what will be hot new electronics products in 2013 that we should be designing now.

PP

ANALOG INTEROPERABILITY: WHAT'S THE ROI?
Wednesday, June 16 3:30 - 4:15pm

Business

Chair: **Rahul Goyal -** *Intel Corp., Santa Clara, CA*
Organizer: **Jan Willis -** *Calibra Consulting, Bracknell, United Kingdom*

Speakers:
James Lin - *National Semiconductor Corp., Santa Clara, CA*
Tom Quan - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*
Mark Waller - *Pulsic Ltd., Bristol, United Kingdom*

Interoperability of EDA tools has always been a complex subject, especially when it comes to analog and mixed-signal design solutions. Does the lack of standards prevent tool innovation and automation? Are interoperable PDKs necessary? Who benefits the most? Users and vendors will discuss the issues and solutions.

PP

SOC VERIFICATION: ARE WE THERE YET?
Wednesday, June 16 4:30 - 5:15pm

Verification and Test

Chair: **JL Gray** - *Verilab, Inc., Austin, TX*
Organizer: **Richard Nordin** - *Breker Verification Systems, Inc., Austin, TX*

Speakers:
John Goss - *IBM Corp., Raleigh, NC*
Rowland Reed - *Qualcomm, Inc., Austin, TX*
Dave Whipp - *NVIDIA Corp., Santa Clara, CA*

Top-down verification cannot find low-level bugs, while bottom-up methodologies cannot stitch together top-level interactions. There are many ways to approach SOC verification but all of them have tradeoffs. Which method should you use for your design? How much verification is enough? This panel will discuss verification methodologies for SOC designs and their requirements for the future.

EXHIBITOR FORUM
EXHIBIT HALL B, BOOTH #1562

EF ANALOG DESIGN ISSUES
Monday, June 14 10:15am - 12:15pm

Analog/Mixed-Signal/RF Design

Tanner EDA / IC Mask Design Ltd.: High Performance Device and Structure Generation for A/MS Design

Attempts to automate the analog layout process have had limited success. Forgoing full automation, Tanner EDA and IC Mask Design focus on acceleration and semi-automation. We will demonstrate that -- without any change to design flow, using only manufacturing design rules -- HiPer DevGen generates high quality design primitives, matched to address common processing artifacts. Results are equal to hand design. Cycle time is dramatically reduced. Users retain control for tuning the design to address specific matching, parasitic and performance requirements.

Speaker:
Ciaran Whyte - *IC Mask Design Ltd., Limerick, Ireland*

Tanner EDA: Challenges and Opportunities Related to PDKs for Analog Design

Process Design Kits (PDKs) are considered an essential enabler to accelerating Analog & Mixed Signal design cycles. Maintaining the integrity of electrical and physical model data across key constituents (foundries, EDA vendors, and designers) requires extensive coordination and ongoing investment. Recent initiatives within the industry to define PDK standards are aimed at addressing the proliferation of unique PDK support requirements. This panel discussion will explore the challenges and opportunities related to PDKs with a focus on Analog Design.

Speaker:
Massimo Sivilotti - *Tanner EDA, Monrovia, CA*

Cadence Design Systems, Inc.: A Methodology for Realizing the Next Generation of Mixed-Signal Designs

For today's mixed-signal SOCs to be profitable, semiconductor companies have to meet a combination of speed, low-power, and yield specifications that set the bar at a whole new level. To meet market demand, companies must also deliver these SOCs under increasingly aggressive schedules. Cadence will discuss a methodology for realizing mixed-signal designs that provides cross-domain interoperability, allows analog and digital designers to improve their productivity throughout the chip design, verification, and implementation process, and ensures that companies will meet their product specification and schedule targets.

Speaker:
Sandy Mehndiratta - *Cadence Design Systems, Inc., San Jose, CA*

EF VERIFICATION TOOLS/METHODOLOGIES
Monday, June 14 2:00 - 4:00pm

Verification and Test

Cadence Design Systems, Inc.: Solutions for IP Exploration and Integration

Utilizing both external and internal IP and design reuse in SOC development is central to reducing cost and risk. However, the selection and integration of IP introduces many new challenges that potentially add to design cost and risk in unexpected ways. In this presentation we will examine these challenges and discuss ways in which they can be avoided and managed.

Speaker:
Neil Hand - *Cadence Design Systems, Inc., San Jose, CA*

Real Intent, Inc.: Efficient and Practical Prevention of X-Related Bugs

It is painful and time consuming to identify X sources and chase their propagation between RTL and Gate representations. Such "X-Prop" issues often lead to a dangerous masking of real bugs. No clear solution has existed thus far to address this problem effectively. This presentation explains the common sources of X's and shows how they can cause functional bugs. It then discusses the challenges that Real Intent has overcome in developing an efficient solution to assist designers in catching bugs caused by X propagation and ensuring X-robust designs.

Speaker:
Oren Katzir - *Real Intent, Inc., Sunnyvale, CA*

FishTail Design Automation, Inc.: Formal Verification of Multi-Cycle Paths on SOCs

Multi-cycle paths are routinely used to meet area, power and timing objectives on high-performance designs. Frequently, however, these constraints are specified incorrectly, either because they apply to paths where they should not, or because there simply is no multi-cycle behavior because of a design bug. Catching these mistakes early is key to silicon success. Failure to do so has serious ramifications - silicon failure, schedule slip. We present a flow for the scalable verification of MCPs on large designs, with an intuitive debug environment and a goal of 100% signoff prior to tapeout.

Speaker:
Ajay Daga - *FishTail Design Automation, Lake Oswego, OR*

EF EMULATION, ESL AND FPGAS
Tuesday, June 15 1:00 - 3:00pm

System-Level and Embedded

EVE-USA, Inc.: Integrating RTL Sub-Systems and ESL Virtual Platforms with ZeBu-Server

Electronic-System Level virtual platforms enable early software development for System-On-Chip designs, but lack the accuracy of hardware models. Register Transfer Level (RTL) simulators are well-suited for hardware verification and can provide accuracy to a virtual platform, but at the cost of performance. ZeBu-Server is an RTL emulator that provides multi-MHz performance, simulator-like debug capabilities, and a transaction-based interface ideal for integration with virtual platforms, creating environments suitable for early software and firmware development, improved hardware verification, and hardware/software co-verification.

Speaker:
Ron Choi - *EVE-USA, Inc., Toronto, ON, Canada*

CoWare, Inc. / Synopsys, Inc.: Software Centric, System-Level Power Optimization for Android Using Synopsys Virtual Prototyping

The Android software platform opens mobile devices such as Smartphones to a worldwide community of open source software developers. While users clearly benefit, what is the impact on power and battery life? Power efficiency is becoming a key issue for software developers, and important quality criteria for their software. This presentation introduces powerful methods for software-centric, system-level power optimization using a Synopsys Virtual Prototype example of the ARM RealView Versatile Platform Baseboard running Android to evaluate and improve power efficiency.

Speaker:
Achim Nohl - *Synopsys, Inc., Aachen, Germany*

Synfora, Inc.: PICO Extreme C Synthesis With Architecture Analyzer

Time consuming verification and early software development requirements are driving SOC designers to high level design methodologies. Using C/C++ provides a1000x gain in simulation performance while simultaneously providing models for early software development. The high level of abstraction of untimed sequential C/C++ descriptions facilitates rapid exploration of hardware architectures but analysis of multiple alternatives can be complex. Synfora's new Architecture Analyzer™ solves this problem using what-if scenarios and rapid visualization of data flows, parallelism and performance.

Speaker:
Vinod Kathail - *Synfora, Inc., Mountain View, CA*

EXHIBITOR FORUM
EXHIBIT HALL B, BOOTH #1562

SI AND EM ANALYSIS
Tuesday, June 15 3:15 - 4:30pm

Interconnect and Reliability

Apache Design Solutions, Inc.: Chip-Package-System (CPS) Co-Design/Co-Analysis using Chip Power Model (CPM)

Meeting system performance specifications at the lowest design and material cost requires an integrated analysis and verification methodology that targets power and signal integrity in a co-design framework. This presentation discusses the requirements, techniques, and methodologies for chip-package-system co-design/co-analysis. It focuses on key aspects of system modeling, extraction, and simulation using electro-magnetic (EM) tools, methods of accurate and distributed modeling of the IC with CPM, and techniques for performing time-domain and frequency-domain simulations for both power and signal integrity issues.

Speaker:
Bhavana Thudi - *Apache Design Solutions, Inc., San Jose, CA*

Apache Design Solutions, Inc.: Reliability Verification for the Post 45nm Era

Shrinking geometries and higher chip performance increases reliability verification complexities across IC, package, and system engineers. Electro-migration requirements and power noise susceptibility are at the forefront of these challenges. Advanced technologies require EM checks to cover transient current flow in wires and vias. Signal-line EM checks need to include average, RMS and peak limit violations to ensure that the devices meet operational lifetime requirements. This presentation will discuss early design planning and analysis flow for mitigating the various reliability risks confronting an IC.

Speaker:
Arvind Shanmugavel - *Apache Design Solutions, Inc., San Jose, CA*

DESIGN FLOW INNOVATIONS
Wednesday, June 16 1:00 - 3:00pm

Low-Power Design

Apache Design Solutions, Inc.: RTL Design for Power Using PowerArtist-XP

Ever-increasing complexity, coupled with the drive towards energy-efficient applications, create a formidable challenge to reduce power. Design decisions made at higher levels of abstraction, such as RTL, have the most significant impact on power. A Design for Power methodology beginning at RTL includes tradeoff analysis for micro-architectural decisions, "power debug" to isolate conditions causing excessive power consumption, application of analysis-driven power reduction techniques for RTL power refinement, and rigorous power regressions at full-chip level to ensure power efficiency of the entire design.

Speaker:
William Ruby - *Apache Design Solutions, Inc., San Jose, CA*

Extreme DA: GoldTime Parametric OCV: A Practical Approach to Statistical STA

Today, On Chip Variation (OCV) deratings are applied to all paths in a design regardless of path depth. Derate values are optimistic for short paths and conservative for long paths. GoldTime, Parametric On Chip Variation (POCV,) can calculate slack variation on any path without full statistical STA libraries. POCV takes the guesswork out of deriving OCV values by reducing the amount of user input to the variation of a single cell stage. We present an overview of the process and results.

Speaker:
Ruben Molina - *Extreme DA Corp., Santa Clara, CA*

FishTail Design Automation, Inc.: Cutting Place & Route Run-Time in Half by Automatically Merging Multi-Mode Constraint Files

Multi-mode place and route does not scale linearly with an increase in design modes. Often, if there are more than two or three design modes run-time and memory usage increases unacceptably. Reverting to dominant single-mode place and route is impractical because it requires iterative ECO loops to converge on timing across all design modes. We present an automated flow for the creation of a merged super-mode constraint file from individual multi-mode constraints. On real customer designs this flow has demonstrated a 50% reduction in place-and-route run-time with no impact to QoR.

Speaker:
Ajay Daga - *FishTail Design Automation, Lake Oswego, OR*

VERIFICATION ADVANCES
Wednesday, June 16 3:15 - 4:30pm

Rm: Exhibit Hall B - Booth #1684

Verification and Test

Amiq Consulting S.R.L.: The DVT IDE for Efficient e and SystemVerilog Development

The DVT™- Design and Verification Tools, an Eclipse-based integrated development environment (IDE), is a modern and powerful, yet easy to use programming platform for e and SystemVerilog verification languages. It enables efficient code writing and simplifies the maintenance of reusable libraries and legacy code. Incorporating advanced code editing features and innovative capabilities specific to functional verification, as well as integrating with all major simulators and the latest verification methodologies, the DVT IDE helps you be more productive and get faster to market.

Speaker:
Cristian Amitroaie - *AMIQ srl, Bucharest, Romania*

GateRocket, Inc.: Breaking the Vicious Cycles in FPGA Verification and Debugging

GateRocket is the only company specifically addressing the increasing challenge of verifying and debugging complex FPGAs. Its unique Device Native® approach verifies the design using the targeted FPGA device in its RocketDrive® verification system, saving weeks in the debug lab, eliminating many costly synthesis-place-route iterations, and reducing FPGA bring-up time by 50% or more. The RocketDrive and its accompanying software debug tool, RocketVision®, turn an existing HDL simulator into a powerful and efficient FPGA debugging system that provides unprecedented visibility into designs and dramatically reduce the 'vicious cycles' of traditional FPGA design approaches.

Speaker:
David Orecchio - *GateRocket, Inc., Bedford, MA*

Date / Time / Rooms

8:00 :15 :30 :45 9:00 :15 :30 :45 10:00 :15 :30 :45 11:00 :15 :30 :45 12:00 :15 :30 :45 1:00 :15 :30 :45 2:00 :15 :30 :45 3:00 :15 :30 :45 4:00 :15 :30 :45 5:00 :15 :30 :45 6:00 :15 :30

RM: 304A FRIDAY, JUNE 11-SATURDAY, JUNE 12 - IEEE INTERNATIONAL HIGH LEVEL DESIGN VALIDATION AND TEST WORKSHOP (HLDVT 2010)

Sunday, June 13

- 207AB: DAC WORKSHOP ON SYNERGIES BETWEEN DESIGN AUTOMATION AND SMART GRID
- 205AB: Begins @ 7:30am | INTERNATIONAL SYMPOSIUM ON HARDWARE-ORIENTED SECURITY AND TRUST (HOST)
- 206A: DAC WORKSHOP ON SYNERGIES BETWEEN DESIGN AUTOMATION AND SMART GRID
- 207D: 8TH IEEE SYMPOSIUM ON APPLICATION SPECIFIC PROCESSORS (SASP 2010)
- 209AB: MULTIPROCESSOR SYSTEM-ON-CHIP (MPSOC): PROGRAMMABILITY, RUN-TIME SUPPORT AND HARRDWARE PLATFORMS FOR HIGH PERFORMANCE APPLICATIONS AT DAC
- 210AB: DAC WORKSHOP ON DIAGNOSTIC SERVICES IN NETWORK-ON-CHIPS (DSNOC) - 4TH EDITION
- 208AB: SYSTEM AND SOC DEBUG INTEGRATION AND APPLICATIONS
- 207C: DESIGN FOR MANUFACTURABILITY COALITION WORKSHOP -"A NEW ERA FOR DFM"
- Hilton Anaheim: NORTH AMERICAN SYSTEMC USERS GROUP (NASCUG 13 MEETING) | ends 7:30pm

Monday, June 14

- 205AB: Begins @ 7:30am | INTERNATIONAL SYMPOSIUM ON HARDWARE-ORIENTED SECURITY AND TRUST (HOST)
- 207D: 8TH IEEE SYMPOSIUM ON APPLICATION SPECIFIC PROCESSORS (SASP 2010)
- 303C: IWBDA: INTERNATIONAL WORKSHOP ON BIO-DESIGN AUTOMATION AT DAC
- 207AB: 4TH IEEE INTERNATIONAL WORKSHOP ON DESIGN FOR MANUFACTURABILITY AND YIELD (DFM&Y)
- 206A: DAC WORKSHOP ON "MOBILE AND CLOUD COMPUTING"
- 208AB: CHOOSING ADVANCED VERIFICATION METHODS: SO MANY POSSIBILITIES, SO LITTLE TIME
- Booth #1562: ANALOG DESIGN ISSUES; VERIFICATION TOOLS/METHODOLOGIES
- 204B: DAC WORKSHOP: MORE THAN CORE COMPETENCE...WHAT IT TAKES FOR YOUR CAREER TO SURVIVE, AND THRIVE! HOSTED BY WOMEN IN ELECTRONIC DESIGN (WWED)
- 207C: ADVANCES IN PROCESS DESIGN KITS WORKSHOP
- 209AB: ESL DESIGN AND VIRTUAL PROTOTYPING OF MPSOCs
- 210CD: LOW-POWER FROM A TO Z
- Booth #694: GARY SMITH ON EDA: TRENDS AND WHAT'S HOT AT DAC; THE MULTIPLIER EFFECT: DEVELOPING MULTICORE, MULTI-OS APPLICATIONS; CAREER OUTLOOK: JOB MARKET 2010; OUTSOURCING DOESN'T MEAN OFF-SHORING— WHAT IS IT? AND, WHY DO IT?; EDA HERITAGE - MEET VERILOG INVENTOR DR. MOORBY AND FORMAL VERIFICATION PIONEER PROF. BRYANT; A CONVERSATION WITH THE 2010 MARIE PISTILLI AWARD WINNER

Tuesday, June 15

- 303C: IWBDA:INTERNATIONAL WORKSHOP ON BIO-DESIGN AUTOMATION AT DAC
- 205AB: NASA/ESA CONFERENCE ON ADAPTIVE HARDWARE AND SYSTEMS (AHS-2010)
- Booth #1562: EMULATION, ESL, AND FPGAS; SI AND EM ANALYSIS
- 204C: MANAGEMENT DAY
- 303AB: ADJUNCT EVENT - CEDA: "BEYOND VON NEUMANN COMPUTING"
- 204AB: ACM STUDENT RESEARCH COMPETITION
- 207AB: 1 EDA CHALLENGES AND OPTIONS: INVESTING FOR THE FUTURE; 7 BRIDGING PRE-SILICON VERIFICATION AND POST-SILICON VALIDATION; 13 WHO SOLVES THE VARIABILITY PROBLEM?
- 209AB: KEYNOTE ADDRESS: BALLROOM ABC — FROM CONTRACT TO COLLABORATION: DELIVERING A NEW APPROACH TO FOUNDRY — DOUGLAS GROSE, *GLOBALFOUNDRIES, SUNNYVALE, CA, PLATFORM, TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.*; 2 POST-SILICON VALIDATION OR AVOIDING THE $50 MILLION PAPERWEIGHT; 8 VIRTUALIZATION IN THE EMBEDDED SYSTEMS: WHERE DO WE GO?; 14 JOINT DAC/IWBDA SPECIAL SESSION - ENGINEERING BIOLOGY: FUNDAMENTALS AND APPLICATIONS
- 207D: 3 SPEED UP YOUR MODEL! RTL, DATA-FLOW, OR SYSTEMC; 9 MEMORY AND MULTIPROCESSOR DESIGN SPACE EXPLORATION; 15 RELIABILITY AND INTEGRITY OF CIRCUITS AND SYSTEMS
- 207C: 4 EMBEDDED SOFTWARE TIMING MATTERS!; 10 INTERCONNECT NETWORKS: PRESENT AND FUTURE; 16 EMBEDDED HARDWARE FOR SECURITY, DATA TYPE REFINEMENT, AND ARBITRATION
- 210AB: 5 THERMAL TRACKING, MONITORING AND CHARACTERIZATION; 11 CORE TECHNIQUES IN FORMAL VERIFICATION; 17 STATISTICAL TECHNIQUES FOR SILICON-TO-MODEL CORRELATION
- 210CD: 6 ADVANCED CLOCK DESIGN AND FLIP-CHIP LAYOUT; 12 NEW FRONTIERS IN ROUTING; 18 PLACEMENT: FROM TRADITIONAL TECHNIQUES TO NOVEL CIRCUIT STYLES
- 2nd Floor: 2U USER TRACK POSTER SESSION
- 208AB: 1U TIMING IS EVERYTHING; 3U FRONT-END DESIGN EXPERIENCES; 4U TAMING BACK-END VERIFICATION AND DFM
- Booth #694: HOGAN'S HEROES: WHAT DESIGN AND LITHOGRAPHY NIGHTMARES WILL 22nm BRING?; EVERYONE LOVES A TEARDOWN (VIRAGE LOGIC); IS THE FPGA TOOL OPPORTUNITY AN OASIS OR A MIRAGE?; 28nm AND BELOW: SOC DESIGN ECOSYSTEM AT A CROSSROAD; HOT AND SPICEY: USERS REVIEW DIFFERENT FLAVORS OF SPICE AND FAST SPICE

Wednesday, June 16

- 205AB: NASA/ESA CONFERENCE ON ADAPTIVE HARDWARE AND SYSTEMS (AHS-2010)
- Booth #1562: DESIGN FLOW INNOVATIONS; VERIFICATION ADVANCES
- 204AB: ACM STUDENT RESEARCH COMPETITION
- 207AB: 19 3-D STACKED DIE: NOW OR THE FUTURE?; 25 DOES IC DESIGN HAVE A FUTURE IN THE CLOUDS?; 31 WHAT'S COOL FOR THE FUTURE OF ULTRA-LOW-POWER DESIGNS?
- 209AB: 20 A DECADE OF NOC RESEARCH - WHERE DO WE STAND?; 26 THE ANALOG MODEL CRISIS – HOW CAN WE SOLVE IT?; 32 DESIGN CLOSURE FOR RELIABILITY; 13TH ANNUAL PHD FORUM AND MEMBER MEETING 6:00 - 7:30pm Rm: 204AB
- 207D: 21 EXPLOITING CONCURRENCY FOR SYSTEM-LEVEL PERFORMANCE; 27 APPLICATION-DRIVEN NETWORK-ON-CHIP DESIGN; 33 ENERGY-EFFICIENT EMBEDDED HARDWARE DESIGN AND MANAGEMENT
- 207C: 22 DATA ACCESS TIMES DEFINE PERFORMANCE!; 28 EXPLOITING FPGA-SPECIFIC FEATURES FOR ROBUSTNESS AND EFFICIENCY; 34 PARALLEL AND EFFICIENT TECHNIQUES IN CIRCUIT SIMULATION
- 210AB: 23 TOOLS FOR EFFECTIVE POST-SILICON VALIDATION AND TEST; 29 LEAKAGE ESTIMATION AND OPTIMIZATION; 35 THERMAL MANAGEMENT AND OPTIMIZATION
- 210CD: 24 SHAPES AND STATISTICS: MANUFACTURABILITY AND YIELD; 30 LOGIC SYNTHESIS IS ALIVE AND KICKING; 36 CATCH OF THE DAY IN BENCHMARKING AND OPTIMAL SYNTHESIS
- 2nd Floor: 6U USER TRACK POSTER SESSION
- 208AB: 5U CASE STUDIES IN FORMAL VERIFICATION; 7U CORNERED: DEALING WITH VARIABILITY; 8U FRONT-END TESTING AND VERIFICATION
- Booth #694: LUCIO'S LITMUS TEST: IS YOUR START-UP READY FOR THE 21ST CENTURY?; IP COMMERCIALIZATION: BEYOND THE CODE; KEYNOTE ADDRESS: BALLROOM ABC — ECHOES OF DAC'S PAST: FROM PREDICTION TO REALIZATION, AND WATTS NEXT? — BERNARD MEYERSON, *IBM Corp., Yorktown Hts., NY*; HIGH-SCHOOL PANEL: YOU DON'T KNOW JACK!; ANALOG INTEROPERABILITY: WHAT'S THE ROI?; SOC VERIFICATION: ARE WE THERE YET?

Thursday, June 17

- 205AB: NASA/ESA CONFERENCE ON ADAPTIVE HARDWARE AND SYSTEMS (AHS-2010)
- 303A: DAC EMBEDDED/SOC ENABLEMENT DAY: EMBEDDED SYSTEMS MEET HARDWARE
- 207AB: 37 DESIGNING THE ALWAYS-CONNECTED CAR OF THE FUTURE; 49 WHAT INPUT LANGUAGE IS THE BEST CHOICE FOR HIGH-LEVEL SYNTHESIS (HLS)?
- 209AB: 38 WACI: WILD AND CRAZY IDEAS; 44 CYBER-PHYSICAL SYSTEMS DEMYSTIFIED; 50 COMPUTING WITHOUT GUARANTEES
- 207D: 39 ALGORITHMS AND ARCHITECTURES FOR EMERGING TECHNOLOGIES; 45 APPLICATION AND IMPROVEMENT OF DYNAMIC VERIFICATION; 51 DESIGN AND MODELING OF TECHNOLOGIES BEYOND CMOS
- 207C: 40 SIMULATION AND MODELING TECHNIQUES FOR DEVICES AND INTERCONNECT; 46 TIMING ANALYSIS AND CIRCUIT OPTIMIZATION FOR NOVEL TECHNOLOGIES AND DFM; 52 YIELD-AWARE OPTIMIZATION AND MODELING FOR ANALOG CIRCUITS
- 210AB: 41 DESIGN OF ULTRA-LOW-POWER SYSTEMS; 47 SYSTEM POWER MODELING AND MANAGEMENT; 53 REDUCING THE COST OF TEST
- 210CD: 42 VARIATION-AWARE METHODS FOR SRAMs AND CLOCKS; 48 MANAGEMENT OF POWER INTEGRITY AND CIRCUIT RELIABILITY; 54 SMART POWER: FROM YOUR CELL PHONE TO YOUR HOME
- 2nd Floor: 10U USER TRACK POSTER SESSION
- 208AB: 9U POWER DELIVERY FROM PACKAGE TO CHIP; 11U JOINT USER TRACK PANEL (SESSION 43) - WHAT WILL MAKE YOUR NEXT DESIGN EXPERIENCE A MUCH BETTER ONE?; 12U ADVANCES IN SYSTEM-LEVEL DESIGN AND SYNTHESIS
- KEYNOTE ADDRESS: BALLROOM ABC — DESIGNING THE MOTOROLA DROID — IQBAL ARSHAD, *Motorola, Inc., Libertyville, IL*

Friday, June 18

- 205AB: NASA/ESA CONFERENCE ON ADAPTIVE HARDWARE AND SYSTEMS (AHS-2010)
- 204C: IEEE/ACM INTERNATIONAL SYMPOSIUM ON NANOSCALE ARCHITECTURES (NANOARCH'10)
- 210AB: SYSTEMC FOR HOLISTIC SYSTEM DESIGN WITH DIGITAL HARDWARE, ANALOG HARDWARE, AND SOFTWARE
- 210CD: 3-D: NEW DIMENSIONS IN IC DESIGN
- 209AB: HOW TO WRITE BETTER SOFTWARE
- Univ. of Irvine: FRIDAY, JUNE 18 - SUNDAY, JUNE 20: 19TH INTERNATIONAL WORKSHOP ON LOGIC AND SYNTHESIS (IWLS)

Topic Area Legend:

- Keynotes
- Exhibitor Forum
- DAC Pavilion
- Panels
- Research Sessions
- Special Sessions
- User Track
- Tutorials
- Workshops
- Colocated
- Misc.

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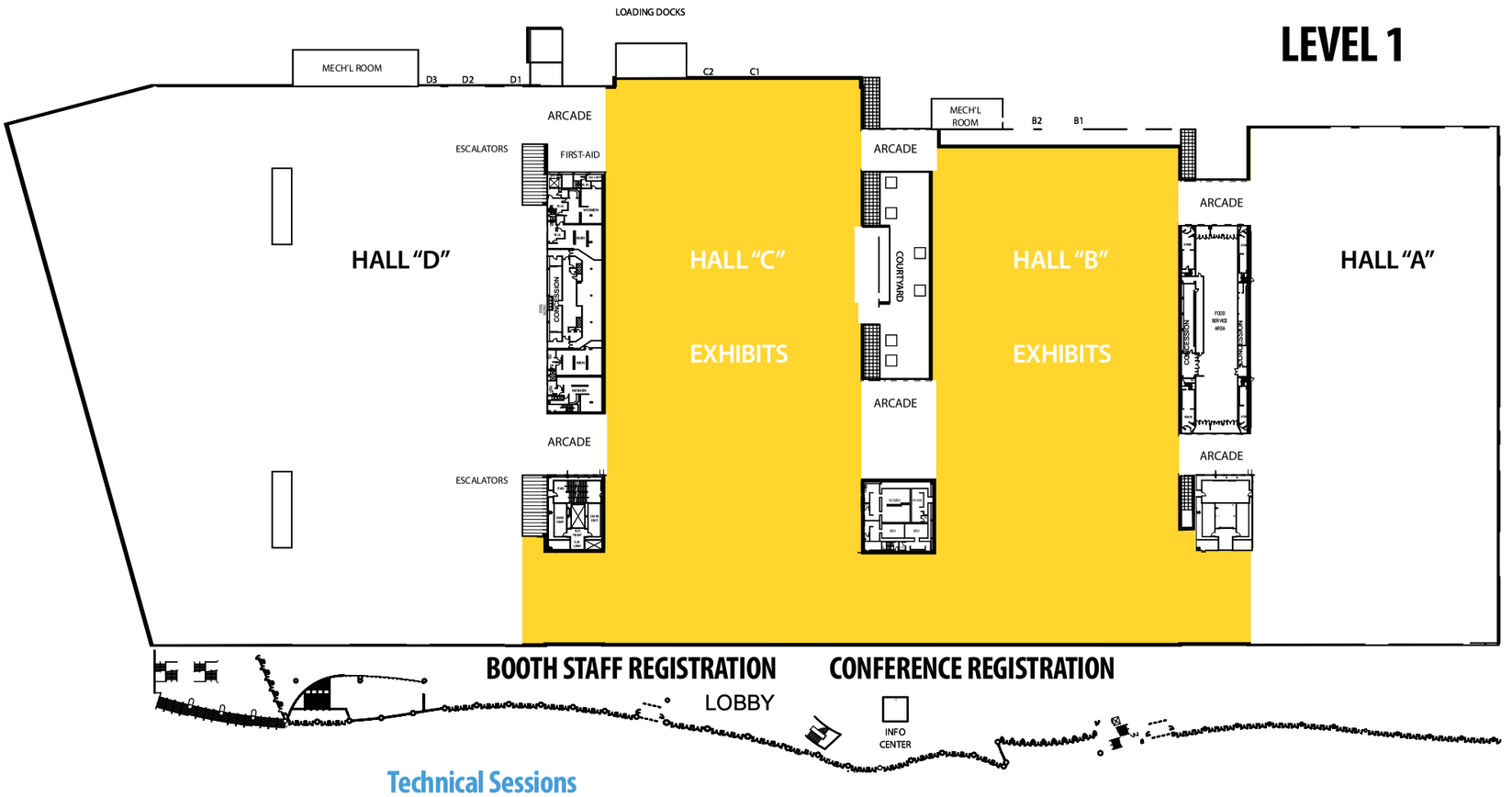

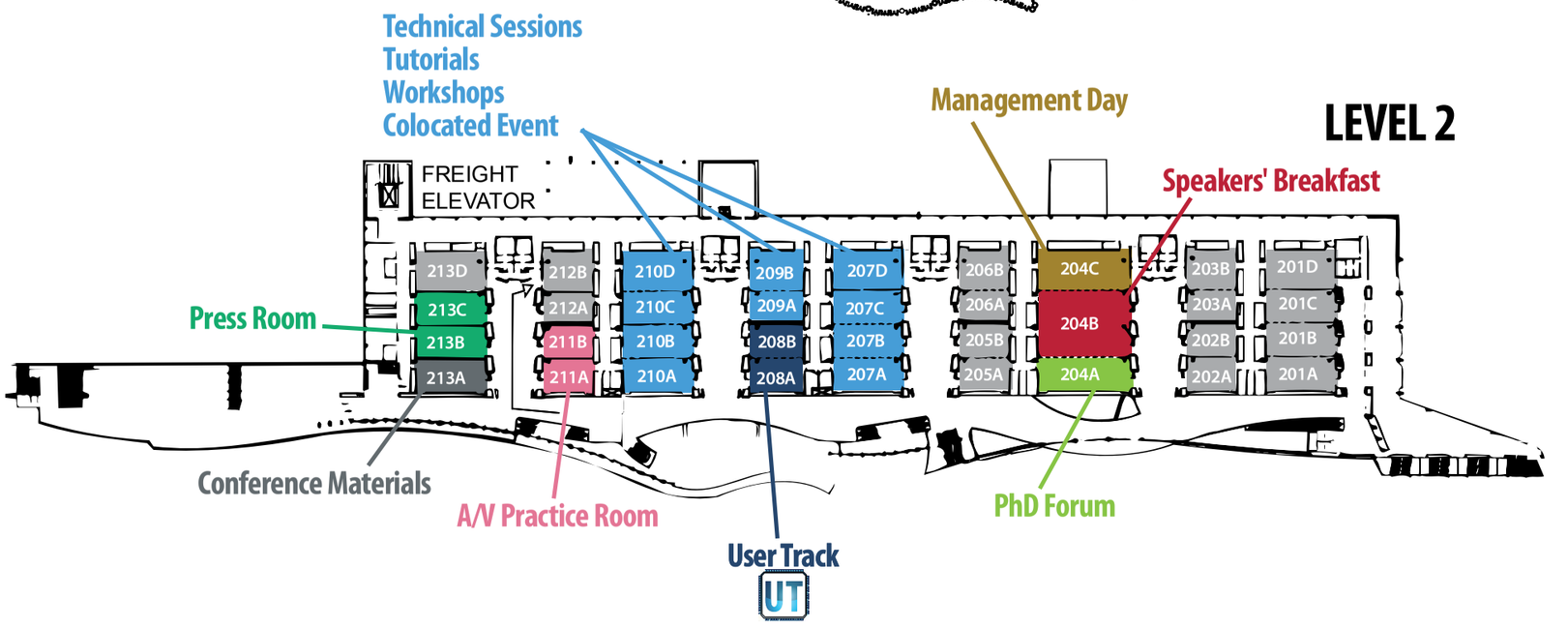

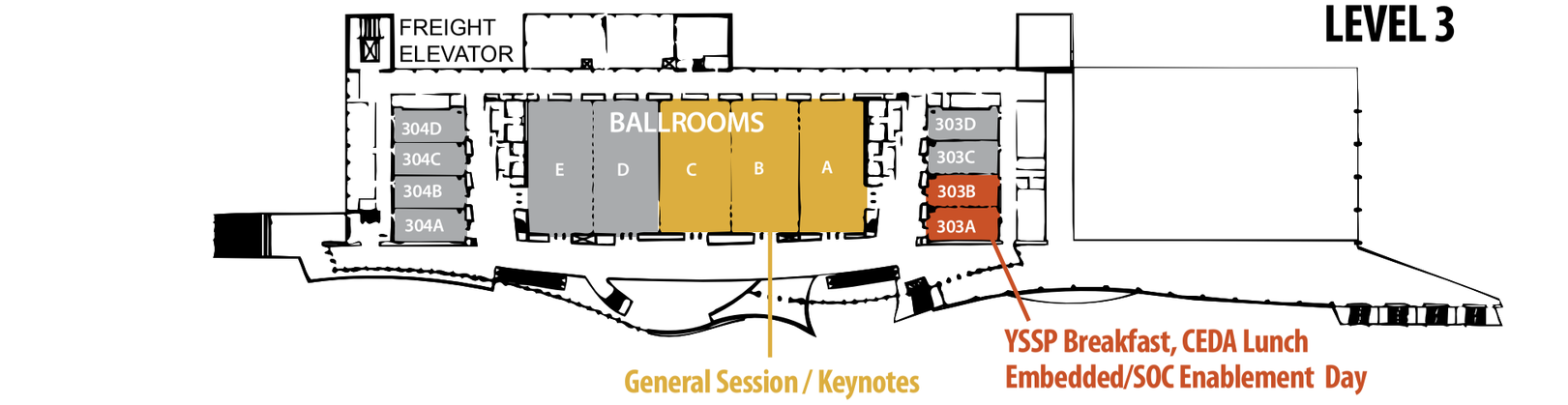

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No Children under the age of 14 are allowed on the Exhibit Floor

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X-FAB Semiconductor Foundries 1408
XJTAG 268
XYALIS 162
Z Circuit Automation 470, 462
Zocalo Tech, Inc. 1509, 1503

IC DESIGN CENTRAL PARTNER PAVILION

EXHIBIT HALL B - BOOTH #1710

AMIQ CONSULTING S.R.L.: THE DVT INTEGRATED DEVELOPMENT ENVIRONMENT FOR e AND SYSTEMVERILOG

Monday, June 14 10:30 - 11:00am

System-Level and Embedded

The DVT™- Design and Verification Tools, an Eclipse-based integrated development environment (IDE), is a modern and powerful, yet easy to use programming platform for e and SystemVerilog verification languages. It enables efficient code writing and simplifies the maintenance of reusable libraries and legacy code. Incorporating advanced code editing features and innovative capabilities specific to functional verification, as well as integrating with all major simulators and the latest verification methodologies, the DVT IDE helps you be more productive and get faster to market.

IBM CORP.: THE INSIDE STORY ON IBM'S PRODUCT DEVELOPMENT TRANSFORMATION

Monday, June 14 11:00 - 11:30am

System-Level and Embedded

IBM Systems and Technology Group designs and manufactures a wide spectrum of products, from chips and boards through mainframes and supercomputers along with their associated firmware. By standardizing on IBM Rational's change management solution for over 18,000 users dispersed across the globe, IBM has been able to transform its product development capability and enable its hardware and software engineers to develop complex products in parallel, improving both quality and time to market. This session explores IBM's hardware and software co-development journey and discusses the benefits realized.

BEECUBE, INC.: REAL-SPEED PROTOTYPING – BEE3

Monday, June 14 11:30am - 12:00pm

Verification and Test

BEEcube provides a High-Speed multiple FPGA prototyping and verification platform. With over 150 BEE systems purchased world-wide, BEEcube will present BEE3 technology targeting:

- Computation/Algorithm prototyping
- SOC/IP RTL verification
- SOC/CPU architecture exploration

BEE3's symmetrical Honeycomb™ architecture, coupled with high-speed Sting I/O™, local monitoring and control with the Nectar OS ™, industry's largest Trace memory, was used in verifying CPUs for Sun, and computer architecture for Microsoft, as well as numerous wireless, networking, consumer electronic and video/audio design validation.

GARY STRINGHAM & ASSOCIATES, LLC: CONQUERING HARDWARE/FIRMWARE INTEGRATION CHALLENGES

Monday, June 14 12:00 - 12:30pm

System-Level and Embedded

Your engineers are trying to integrate firmware (a.k.a. embedded software) with hardware but there are problems. At times, it is unknown if the problem is on the hardware side or the firmware side. Or the problem is known but the solution requires a major firmware change or a hardware respin, each of which delays introduction and increases costs. This presentation teaches what to do to eliminate or mitigate these problems, enabling you to produce a quality product.

ASIC ANALYTIC, LLC: ASIC ANALYTIC

Monday, June 14 12:30 - 1:00pm

Verification and Test

ASIC Analytic will be presenting an overview of who we are, our unique network attached box and explain how it will improve ASIC design productivity. Customer examples will be presented. We will also contrast how our technology and ease of use compares to the typical EDA software model. We will be backing up our claim of superior ease of use by giving out free pass cards good for a month.

X-FAB SEMICONDUCTOR FOUNDRIES: CMOS AND MEMS INTEGRATION: NEW STRATEGIES IN COST/PERFORMANCE

Monday, June 14 1:00 - 1:30pm

General Interest

In complex electro-mechanical systems, CMOS/MEMS integration offers many potential benefits – smaller packaging, lower cost, and minimization of part count through higher levels of component integration. Initial implementations of leading products in this market segment relied on discrete electrical and MEMS subsystems (e.g., MEMS microphones, accelerometers, etc.). This presentation explores the integration of CMOS-based electrical subsystems with MEMS components on the same substrate, including available manufacturing process capabilities, design flows, limitations and potential cost/benefit impacts.

R3 LOGIC INC.: 3-D IC - PACKAGE CO-DESIGN WITH R3INTEGRATOR™

Monday, June 14 1:30 - 2:00pm

General Interest

Designing 3-D integrated systems with optimal re-use of existing IP libraries poses a variety of unique challenges. There are multiple choices for stacking technologies: via first, via last, via middle, use TSV's or copper bonding, or both; and multiple choices for mixing and matching die technologies. R3Integrator helps you navigate these challenges by providing a true 3-D design environment interacting directly with 3rd-party vendor tools for 2-D IC and package design.

IC DESIGN CENTRAL PARTNER PAVILION

EXHIBIT HALL B - BOOTH #1710

EXPERTIO, INC.: VERIFICATION IP SELECTION CRITERIA

Monday, June 14 2:00 - 2:30pm

Verification and Test

This presentation will cover the criteria that one should use when performing the selection process for Verification IP, along with guidelines and things to consider when using VIP in your simulation environment. The presentation will also touch on industry terminology and common practices with respect to state-of-the-art verification.

AUSDIA, INC.: TOP 4 1/2 PROBLEMS IN TIMING CLOSURE

Monday, June 14 2:30 - 3:00pm

Synthesis and FPGA

In 2009, Ausdia did an extensive research study to get real data on the state of timing closure. We correlated this against several key trends and discovered 4 1/2 critical issues that you need to be aware of to stay successful, and avoid crippling schedule blowouts in timing closure.

Come and hear about the standout issues that came out of the survey, why they are so important to address immediately, and how to solve these problems today.

BEECUBE, INC.: REAL-SPEED PROTOTYPING – BEE3

Monday, June 14 3:00 - 3:30pm

Verification and Test

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CAMBRIDGE ANALOG TECHNOLOGIES: ULTRA-LOW-POWER HIGH PERFORMANCE ANALOG TO DIGITAL CONVERTERS WITHOUT OPERATIONAL AMPLIFIERS

Tuesday, June 15 12:00 - 12:30pm

Low-Power Design

The focus of this talk is on the design of ultra-low-power high performance discrete time analog to digital converters using precision switched capacitor circuits without Operational Amplifiers (PUMA(TM)). These OpAmpless switched capacitor circuits are able to achieve high levels of precision through the use of zero-crossing detectors that detect virtual ground conditions instead of forcing that conditions as in OpAmp based circuits. This talk will describe the zero-crossing based switched capacitor technology and applicability in low power electronics.

X-FAB SEMICONDUCTOR FOUNDRIES: DESIGNING FOR ANALOG/ MIXED-SIGNAL EXTREMES: HIGH-TEMPERATURE / HIGH-RELIABILITY

Tuesday, June 15 12:30 - 1:00pm

General Interest

The real world isn't a very friendly place for semiconductor electronics. Temperatures in automobile engine compartments, for example, routinely exceed 150C, yet may plummet to -40C on frigid winter nights. Designing high-reliability electronic systems for the real world requires optimization for such harsh environments, and unique modeling and simulation support, allowing designers to accurately predict performance and reliability. This presentation identifies specific requirements for such design, and X-FAB's process technologies and unique tool support to fully utilize it.

AVANT TECHNOLOGY, INC.: IP SOLUTIONS FOR SOC

Tuesday, June 15 1:00 - 1:30pm

Physical Design

Today's SOC's requires much work of integrations among the different categories due to the increase of the new applications. Thus, it becomes more important for the SOC designers to choose the IP more efficiently for either achieving their work successfully or also meet the time-to-market. Among the different choices, the solution supporting the different fields will be much more beneficial than the others. In this presentation, we will introduce several IP solutions from the different fields which may support such needs: MIPI, SD/SDIO, USB, Ethernet, connectivity IP, SATA, SRAM-1T, SRAM-6T, ROM, Register File.

ALTAIR ENGINEERING: REDUCE, REUSE, RECYCLE – 21ST CENTURY WORKLOAD SCHEDULING WITH PBS WORKS

Tuesday, June 15 1:30 - 2:00pm

Business

PBS Works is a complete portfolio of software tools for building, managing, and using high-performance computing infrastructure. Reduce your expenses – PBS Professional extracts maximum performance from multicore architectures, reduces power use via Green Provisioning, and enables highly available, highly-scalable Clusters, Grids and Clouds. Reuse your people – PBS Catalyst user portals streamline workflow, freeing EDA engineers from learning (and re-learning) computer-ese, letting them focus on EDA. Recycle your licenses – PBS Analytics graphically identifies hardware and license usage and patterns so you can buy only what you really need.

IC DESIGN CENTRAL PARTNER PAVILION

EXHIBIT HALL B - BOOTH #1710

TSSI - TEST SYSTEMS STRATEGIES, INC.: PRE-SILICON VALIDATION – WHY SOME DESIGNS ALWAYS BEAT THE DEADLINE?

Tuesday, June 15 2:00 - 2:30pm

Verification and Test

Virtual Testing is not a new concept, but it is hardly popular. Most virtual test solutions are really imposing pattern validation tasks onto the design team to re-simulate, or "replay".

The true virtual test platform enables collaboration to save overall time and effort for both design and test teams. TSSI VirtualTest (TVT) users shrink design verification and patterns bring-up time from months to hours. Design bugs are caught before tapeout while 100% test vectors work the first time on silicon.

ENTERPOINT LTD.: USING BROADDOWN5 AS ASIC PROTOTYPING TARGET

Tuesday, June 15 2:30 - 3:00pm

Verification and Test

Enterpoint offers a number of products and services aimed at ASIC and FPGA development markets. Our FPGA based development boards offer a range of solutions ranging from large single chip prototyping solutions to more cost effective solutions using arrays of low cost devices. Custom circuit and PCB design and manufacture are also available. This is backed up by Consultancy, IP Development, Design Rescue and Integration Services that are available to help you to complete your project on time.

CISC SEMICONDUCTOR DES.+CONS. GMBH: SYAD®'S MODULE SIMBA: CONNECTING REQUIREMENTS ENGINEERING WITH SYSTEM DESIGN AND IMPLEMENTATION

Wednesday, June 16 12:00 - 12:30pm

Verification and Test

Being in its 3rd generation the multi HDL design and (co-)simulation framework SyAD® (System Architect Designer) offers now modules for SIMulation Based Analysis of System Requirements (SIMBA).

SyAD®'s module SIMBA is a fully featured simulation based verification environment for Black- and White Box verification.

Automatic generation of test benches based on use cases from the system specification and a Verification Planer provide the perfect overview if requirements are met.

COFLUENT DESIGN: MULTICORE SYSTEM MODELING AND SYSTEMC-BASED SIMULATION WITH UML, SYSML AND MARTE

Wednesday, June 16 12:30 - 1:00pm

System-Level and Embedded

CoFluent Design introduces a new UML methodology for modeling and simulating embedded systems and chips. It combines SysML and MARTE profiles, and is supported by the CoFluent Studio software based on Eclipse. CoFluent Studio allows designers to model real-time applications and use cases, and simulate their execution on multiprocessor/multicore platforms. Simulation allows for behavioral and real-time validation, as well as performance and power prediction. SystemC TLM code is automatically generated from UML models, and can be reused as functional or test case model in verification and virtual platform environments from CoWare, Synopsys, and Mentor Graphics.

ZOCALO TECH, INC.: MAKING LIFE EASIER FOR IP PROVIDERS AND USERS

Wednesday, June 16 1:00 - 1:30pm

Verification and Test

It is well understood that by populating IP with quality assertions, debug and integration issues can be significantly reduced. However, adaption of this strategy has been limited because of the time and knowledge required to rigidly assess where assertions are required and the coding of more useful and powerful assertions.

This presentation discusses how Zocalo Tech's product, Zazz, provides the level of automation required to cost effectively adapt an assertion strategy and make life easier for IP providers and users.

INOCS: NETWORK-ON-CHIP SYNTHESIS

Wednesday, June 16 1:30 - 2:00pm

Physical Design

Current and future SOCs are composed of a large number of IP blocks and are increasingly hard to integrate, due to performance, timing closure, floorplanning, IP heterogeneity, clocking challenges.

iNoCs proposes Network-on-Chips to tackle these issues.

An NOC design tool takes high-level communication requirements as an input and outputs NOC RTL, accounting for wirelength and clocking concerns. Existing IP cores can be seamlessly integrated while matching performance and timing constraints. The iNoCs flow saves design effort and optimizes time-to-market.

ADDITIONAL MEETINGS

AM

KICK-OFF RECEPTION

Sunday, June 13 6:00 - 7:30pm

Rm: Hilton Anaheim

General Interest

AM

INTEROPERABLE PDKS ARE HERE TO STAY: NEW ERA OF ANALOG/CUSTOM INNOVATION

Monday, June 14 11:30am - 1:00pm

Rm: Anaheim Marriott, Marquis North Ballroom

General Interest

At the 4th Annual IPL Luncheon, the IPL Alliance will present IPL 1.0, the industry's first open standard for interoperable PDKs. IPL members and their customers will present iPDK development/validation flows as well as experiences and successes.

Attendees will hear about:

- Challenges, features, qualification procedures and roadmaps of foundry iPDKs
- Experiences using an iPDK
- Industry collaboration status on PDK standard

AM

Rm: 203A

THE ANNUAL SI2 OPEN MEETING

Monday, June 14 6:00 - 7:30pm

General Interest

The Annual Si2 Open Meeting is open to both member and non-member companies and individuals who are interested in Si2 activities such as OpenAccess, advanced library modeling systems, DFM, low-power design and OpenPDK. A networking opportunity will be held at the beginning and end of the meeting with refreshments and light hors d'oeuvres. Steve Schulz, President & CEO of Si2, will present an outline of Si2's activities and accomplishments of the past year and directions for the year ahead, and will also announce the newly-elected members of Si2's Board.

AM

SYNOPSYS PRIMETIME SPECIAL INTEREST GROUP (SIG) RECEPTION

Monday, June 14 6:00 - 8:00pm

Rm: Anaheim Marriott, Grand Ballroom E

General Interest

Synopsys invites you to join us for cocktails, dinner and an informative and interactive session covering the latest variation aware timing analysis trends, challenges and solutions. Listen to industry-leading experts discuss best practices and present their views on the variation aware topics. If you are a timing signoff engineer or manager, you won't want to miss this special event.

AM

SYNOPSYS UNIVERSITY RECEPTION

Monday, June 14 6:30 - 8:00pm

Rm: Anaheim Marriott, Marquis North

General Interest

University professors and students are invited to join Synopsys for an evening reception including drinks and hors d'oeuvres. Prize drawings will be held throughout the evening and the following keynote presentations will be featured.

AM

8TH ANNUAL ESL SYMPOSIUM PANEL

Tuesday, June 15 12:00 - 1:30pm

Rm: Ballroom E

System-Level and Embedded

This panel will discuss the key factors driving companies to adopt ESL design tools and the benefits the tools provide. Six panelists will share their experiences using HW and SW electronic system level design methodologies for multicore, high performance and low power architectures, and give their insight on how to accomplish a predictable and productive design and verification process using ESL.

Lunch will be provided, iPad drawing giveaway.

Speaker:
Walden Rhines - *Mentor Graphics Corp., Wilsonville, OR*

AM

INDUSTRY LEADERS VERIFICATION LUNCHEON

Tuesday, June 15 12:00 - 2:00pm

Rm: Anaheim Marriott, Grand Ballroom Salon E

Verification and Test

Synopsys invites you to join us for lunch and a highly informative session covering the latest verification trends, challenges and solutions. Listen to experts from industry-leading companies discuss best practices and present their views on the hottest verification topics. If you are a verification engineer or manager, you won't want to miss this special event.

ADDITIONAL MEETINGS

CANDE MEETING

AM
Rm: 206B

Tuesday, June 15 5:45 - 7:00pm

Business

BIRDS-OF-A-FEATHER MEETINGS

AM

Tuesday, June 15 6:30 - 8:00pm

General Interest

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF). All BOF meetings are held at the Anaheim Convention Center, Tuesday, June 15 / 6:00 - 7:30pm. DAC will facilitate common interest groups meetings to discuss DA related topics. To arrange a BOF meeting, please sign up at the Information Desk located in the mail lobby. A meeting room will only be assigned if then or more people sign up. An LCD projector and screen will be provided. Check DACnet and the Birds-of-a-Feather board at the information desk.

PROMOTING DAC CONTENT VIA SOCIAL MEDIA

AM
Rm: 209AB

Tuesday, June 15 6:30 - 8:00pm

Business

Organizer: **Shishpal Rawat** - *Intel Corp., Folsom, CA*

We will discuss how social media could be utilized effectively to reach a wider audience. What are the popular mechanisms utilized by DAC professionals and what can be done by DAC organizers to reach them.

INTEROPERABILITY BREAKFAST IN 3-D: SYSTEM-LEVEL AND CUSTOM DESIGN STANDARDS COMING RIGHT AT YOU

AM

Wednesday, June 16 7:30 - 9:30am

Rm: Anaheim Marriott, Marquis Room

System-Level and Embedded

Chi-Foon Chan, President and COO of Synopsys, invites you to attend Synopsys' interoperability breakfast sponsored by HP. See how open system-level standards bridge EDA to embedded software and speed product design. Hear the latest on interoperability benefits for advanced analog design automation. See who wins the Tenzing Norgay Interoperability Achievement Award.

DAC/ISSCC STUDENT DESIGN CONTEST PRESENTATIONS

AM
Rm: 205AB

Wednesday, June 16 3:00 - 4:30pm

General Interest

The purpose of the DAC/ISSCC Student Design Contest is to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. The Student Design Contest is jointly sponsored by DAC and its sponsors, by ISSCC, and by a set of corporate sponsors. The awarded winners will present their projects during this time frame.

TANNER EDA: DRIVING ANALOG INNOVATION

AM
Rm: 202A

Thursday, June 17 8:30 - 11:00am

General Interest

Current and prospective Tanner EDA users are invited to join Greg Lebsack (President) and Mass Sivilotti (CTO) as they share perspectives on the EDA industry, Tanner's business strategy and product roadmap.

The meeting will also include presentations from current users who will share their experience creating Analog ICs and MEMS with Tanner tools.

Learn how Tanner's full-flow product suite is enabling innovations ranging from high-speed I/O devices at deep nanoscale to world-leading image sensors designed for diverse industry applications.

A light breakfast will be served and each registered attendee will receive a chance to win a new Apple iPad. Don't miss this fun, informative and interesting session!

X-FAB SEMICONDUCTOR FOUNDRIES: CHALLENGES OF SOC SENSOR INTEGRATION: EXPLORING LIFE BEYOND PURE DIGITAL CMOS IN THREE USE CASES

AM
Rm: 303C

General Interest

Thursday, June 17 1:30 - 4:00pm

Organizer: **Mark Miller** - *X-FAB Semiconductor Foundries, Santa Clara, CA*

Despite engineering teams' ingenuity and experience, life beyond digital/CMOS – commonly known as "More than Moore" – comes with an undeniable set of complex real-world challenges. Engineers must grapple with economic challenges of making their applications commercially feasible, process integration challenges of dealing with technologies that are incompatible with standard CMOS, and design support challenges of moving beyond traditional standard digital design. This seminar highlights these issues through use cases for three emerging application arenas beyond pure digital CMOS – CMOS/MEMS integration, extreme temperature applications, and high-reliability applications.

Speakers:
Mark Miller, **Paul Poenisch** - *X-FAB Semiconductor Foundries, Santa Clara, CA*
Iain Rutherford, **Olaf Zinke** - *X-FAB Semiconductor Foundries, Erfurt, Germany*

NOTES

DESIGN AUTOMATION CONFERENCE & ISSCC

present

Wednesday, June 16
3:00 - 4:30pm

Sigda University Booth
2nd Level

Student Design Contest

See page 65 for more details...

6 WINNERS!

Thanks to our sponsors:

Mentor Graphics® IEEE CEDA IEEE Council on Electronic Design Automation SYNOPSYS® intel