EXHIBITING COMPANIES

Accelicon Technologies, Inc.
Cupertino, CA
www.accelicon.com Booth: 1321
Accelicon Technologies is the technology leader in device-level modeling and validation. With over 100 customers worldwide, Accelicon has established itself as a clear market leader. Accelicon's products are: MBP, the next-generation device-level model extraction and generation solution, incorporating superior optimization and simulation for 'order of magnitude' performance improvement and unparalleled ease of use, MQA, a rules-driven device-level model validation solution used for model QA and qualification, and PQA automating the analysis of advanced model layout-effects on the design.

ACCIT - New Systems Research
Alexandria, Egypt
www.accit-newsystemsresearch.com Booth: 754
ACCIT - New Systems Research is a total solution provider offering products in the field of Electronic Design Automation tools, implemented on massively parallel multicore/ multiprocessor architectures and GPU accelerators. We offer a massively parallel and scalable transient analysis module, which comes as a part of a full precision true analog SPICE simulator. We are also developing a plug-and-play platform in the form of standardized closed-box software interfaces and hardware setups, offered to EDA companies for parallelizing their own analog simulators.

ACE Associated Compiler Experts bv
Amsterdam, The Netherlands
www.ace.nl Booth: 368
ACE Associated Compiler Experts is one of the world's oldest independent employee-owned IT companies supplying advanced system software products and know-how. With a natural drive to perfection, the compiler experts at ACE are committed to delivering high quality in both products and services. ACE ensures that, the CoSy compiler development system and the SuperTest compiler test and validation suite are recognized for their outstanding quality and support.

Agilent Technologies
Santa Rosa, CA
www.agilent.com Booth: 156
Agilent EEsof EDA (booth #156) is the technology leader and industry's leading supplier of Electronic Design Automation (EDA) software for microwave, RF, high-frequency, high-speed, RF system, electronic system level (ESL), circuit, 3-D electromagnetic, physical design and device-modeling applications. Join Agilent in booth #156 where you can look at the most trusted tools for highly integrated RF circuit simulation and analysis as well as Communications ESL. Come see the latest in:
- GoldenGate RFIC solutions
- SystemVue Communications ESL

Agnisys, Inc.
Lowell, MA
www.agnisys.com Booth: 359
Agnisys provides innovative tools for design and verification of IPs/SoCs targeting ASICs/FPGAs. IDS manages register and memory map information through the product life-cycle. It provides complete data portability in various formats such as RTL, C/C++ headers, OVM/VMM, RALF, IP-XACT, SystemRDL, Word, FrameMaker and more. IVS is an enterprise class, web based verification planning and management tool. It centralizes requirement capture, verification planning, simulation result analysis and bugs. It's a powerful DO-254 enabling tool to close the loop on open-ended-verification. IAS bridges the gap between specification and assertions.

Aldec, Inc.
Henderson, NV
www.aldec.com Booth: 1373
Aldec, Inc. offers SystemVerilog OVM/VMM/UVM methodology support and hardware-assisted verification. Register to attend technical presentations on Advanced Verification Methodologies, Assertion-based Verification, SystemVerilog, HDL Design Rule Checking, Unified Code and Functional Coverage, Hardware Emulation (SCE-MI) and DO-254 Compliance validation. Aldec products, the choice of 30,000 plus engineers, include Active-HDL, Riviera-PRO, ALINT, HES and DO-254 Compliance Tool Set. Register: www.aldec.com/Registration/DAC.

Altair Engineering
Troy, MI
www.altair.com Booth: 1414
The PBS Works(tm) suite of tools allows enterprises to maximize ROI on computing infrastructure assets: making engineers more productive and making infrastructure more efficient, more reliable, and more cost effective. PBS Catalyst(tm) brings 'drag-and-drop' simplicity to job submission; PBS Professional® optimizes use of hardware and expensive software licenses; and PBS Analytics(tm) enables data-driven planning, chargeback, and forecasting. For 25 years, Altair has provided innovative solutions delivering sustained competitive advantages to our 3,000+ customers throughout the world.

Altos Design Automation
San Jose, CA
www.altos-da.com Booth: 1367
Are you ready for more corners? Altos Design Automation (www.altos-da.com) provides ultra-fast, easy to use IP characterization solutions for standard cells, complex I/Os and embedded memory. With Altos' "inside view" technology additional library corners with advanced timing, noise and power (CCS/ECSM) can be created in hours not days. Altos also offers comprehensive library validation and statistical timing model creation. To learn how to "improve your view" and get the additional corners you need fast, visit our booth here at DAC.

EXHIBITING COMPANIES

Amiq Consulting S.R.L.
Bucharest, Romania
www.amiq.ro Booth: 1417

AMIQ is a global company focused on adding value to the verification domain through its proprietary tools and over 10 years of consulting experience spanning ASIC functional verification and reusable Verification IP development. AMIQ develops and markets the Design and Verification Tools (DVT) platform, the first integrated development environment (IDE) for e and SystemVerilog. Designed to maximize verification productivity and quality, the DVT solution enables engineers to complete their projects faster and increase the likelihood of first tape out success. Websites: www.amiq.ro; www.dvteclipse.com Contact: sales@amiq.ro.

AnaGlobe Technology, Inc.
Hsinchu, Taiwan
www.anaglobe.com Booth: 812

AnaGlobe provides Thunder which is a unique layout tool for the final layout stage. It provides full editing/viewing functions of extreme efficiency for huge GDS/OASIS (can also import OpenAccess and LEF/DEF) files. Features:

- System Integration (IP merge)
- Design Consolidation (remove redundant cells)
- Connectivity Tracing (include find-short)
- Design Comparison
- Boolean Operations
- Metal Density Check
- DRC/LVS Results Viewing
- 3D View
- Layout Editing GUI
- Layout Editing API (C++/TCL/Perl/Python)
- Customization/Extension with TCL/Perl/Python

Analog Bits, Inc.
Mountain View, CA
www.analogbits.com Booth: 183

Analog Bits, Inc. specializes in designing transistor level IP components fully customized for easy and reliable integration into modern CMOS digital chips. Products include precision clocking macros such as PLLs, DLLs, programmable interconnect solutions such as multi-protocol SERDES, DDR/programmable I/Os and specialized memories such as high-speed SRAMs, T-CAMs. With billions of IP fabricated in customer silicon from 0.25-um to 28-nm processes, Analog Bits is the premier IP supplier with an outstanding heritage of "first time working silicon" at merchant foundries and IDMs.

Apache Design Solutions, Inc.
San Jose, CA
Gold Exhibitors
www.apache-da.com Booth: 535

Apache provides industry's leading power and noise solutions for chip-package-system convergence from RTL to sign-off. Apache's products address the critical power noise challenges associated with specific design domains such as digital, analog/mixed-signal, package/PCB, and SiP/3D-IC, while providing an eco-platform that integrates the SoC, Custom IP, and System worlds. From RTL power analysis and reduction, to early stage prototyping and optimization, and through chip and package sign-off, Apache's products enable designers to reduce power, increase performance, lower cost and mitigate risk.

Applied Simulation Technology
San Jose, CA
www.apsimtech.com Booth: 557

Applied Simulation Technology is a leader in the area of Electromagnetic modeling and simulation offering innovative solutions for Signal Integrity, Power Integrity and EMI analysis. The software enables engineers to analyze the impact of the layout interconnect and power distribution on system performance. The emphasis this year at DAC will be EMI tools. Early detection of problematic areas are highlighted on the CAD design. High frequency return currents are considered in the analysis.

Artwork Conversion Software, Inc.
Santa Cruz, CA
www.artwork.com Booth: 511

Artwork will be demonstrating our tools for IC and mask designers including the latest Qckvu3 which handles extremely large GDSII and OASIS files - we've reduced the memory footprint and enabled pre-filtering of layers and cells. We've also added a plug-in API enabling users to create their own custom features. Artwork will also be demonstrating our IC plotting software, our CAD translators, our mask boolean tools. "These are suitable for both end users and other EDA companies who wish to incorporate them into their tools. We've recently partnered with AWR to offer intelligent import from Cadence Allegro and from the ODB++ database into Microwave Office. Finally, we've released a new program that can take package drawings in AutoCAD and import them intelligently into Cadence APD/SIP.

ASIC Analytic, LLC
Shakopee, MN
www.asicanalytic.com Booth: 1516

ASIC Analytic offers a complete HDL analysis engine that creates a new standard in both thoroughness and ease of use. 1) Any and all errors, inefficiencies, anomalies, and non-standard circuit topologies are reported to the user in a prioritized graphic. 2) ASICProbe is ready for immediate use.
There are no configuration, setup or technology files of any kind. There are not even any command line options. It is that easy to use! ASICProbe runs on the command with just the desired HDL files.

ATEEDA
Edinburgh, United Kingdom
www.ateeda.com Booth: 1016

New for DAC 2010 - Pushbutton BIST for 16-bit ADCs Following success in volume production, ATEEDA is launching a new 16-bit variant of LinBIST for ADCs at DAC 2010. LinBIST helps all semiconductor companies (whether IDM or Fabless) take advantage of the cost-savings associated with Built In Self Test for ADCs and DACs. ATEEDA's tools use smart algorithms to deliver BIST with restricted digital gates and minimal analog circuitry. ATEEDA. Cutting the cost of analog test.

EXHIBITING COMPANIES

Atoptech
San Jose, CA
www.atoptech.com Booth: 1042

ATopTech was founded by leading EDA physical design implementation experts to build the next generation of place and route tools focused on designs at 65nm and below. Our goal is to provide the fastest turn-around time while providing the best quality of results. AtopTech's products form a complete netlist-to-GDSII physical design solution, from top level design and prototyping to complete block level design while handling all the complexities of variability such as MCMM and AOCV. Excellent correlation with both timing and physical verification sign-off tools is one of our trademark capabilities!

Atrenta Inc.
San Jose, CA
Silver Exhibitors
www.atrenta.com Booth: 744

Atrenta is the leading provider of Early Design Closure® solutions that radically improve the efficiency of integrated circuit design. Using Atrenta's comprehensive tool suite for architectural chip assembly and RTL analysis, customers can create robust and correct designs rapidly, preventing expensive and tedious iterations during the implementation phase. With over 150 customers worldwide, including the world's top 10 semiconductor companies, Atrenta provides the most comprehensive solution in the industry for Early Design Closure. Atrenta, Right from the Start!

Ausdia Inc.
Sunnyvale, CA
www.ausdia.com Booth: 1504

Ausdia's "TimeVision" products help eliminate the iterations, errors, and unpredictability of timing constraint development and timing closure. TimeVision-Constraints accelerates the development, verification and management of timing constraints at the RTL and gatelevel. TimeVision-Convergence provides precise visibility into timing closure bottlenecks, enables seamless timing correlation across the flow, and performs timing ECOs to expedite the closure process. TimeVision is plug-and-play with existing EDA tools, flows and methodologies.

austriamicrosystems
Raleigh, NC
www.austriamicrosystems.com Booth: 349

austriamicrosystems, a leading designer and manufacturer of high performance analog ICs, combines more than 27 years of analog design capabilities and system know-how with its own state-of-the-art manufacturing and test facilities. austriamicrosystems Full Service Foundry is your analog foundry partner focusing on specialty process technologies like RF-CMOS, High-Voltage CMOS, SiGe-BiCMOS and embedded EEPROM processes. With superior support during the design phase, high-end tools and experienced engineers, austriamicrosystems succeeds to be an attractive analog foundry partner especially for fabless design houses.

AutoESL Design Technologies, Inc.
Cupertino, CA
www.autoesl.com Booth: 1577

AutoESL provides software tools and services that dramatically accelerate the design of systems-on-chip (SoCs). Using state of the art compilation technologies, AutoESL's High Level Synthesis offers the industry's best and only unified language support of C, C++ and SystemC, and performs highly effective optimizations resulting in reliable and highest-quality implementation-aware RTL. AutoESL is being adopted for ASIC and FPGA design by the world's leading companies for improving performance, reducing power, speeding up verification and cutting RTL design time by over 75%.

Avant Technology Inc.
Hsinchu, Taiwan
www.avant-tek.com Booth: 1304

Today's SoC's requires much work of integrations among the different categories due to the increase of the new applications. Thus, it becomes more important for the SoC designers to choose the IP more efficiently for either achieving their work successfully or also meet the time-to-market. Among the different choices, the solution supporting the different fields will be much more beneficial than the others. In this presentation, we will introduce several IP solutions from the different fields which may support such needs: MIPI, SD/SDIO, USB, Ethernet, connectivity IP, SATA, SRAM-1T, SRAM-6T, ROM, Register File.

Avery Design Systems, Inc.
Andover, MA
www.avery-design.com Booth: 1363

Avery is a leading provider of intelligent functional verification solutions. Insight simulation-centric, behavioral formal analysis delivers effective early RTL verification with code, FSM, and property reachability and root cause analysis, robust coverage closure and bug hunting methods on design properties and scoreboards, X verification to find non-determinism in reset and low power sequences, and RT-level DFT analysis. Proven VIP for PCI Express, USB, AXI/AHB, and SATA speeds testbench development and compliance verification. SimCluster parallel simulation accelerates RTL and gate-level simulation by 5-10X using industry leading simulators.

Axiom Design Automation
Milpitas, CA
www.axiom-da.com Booth: 479

Axiom will showcase advances to MPSim, the state-of-the-art, industry proven Verilog/SystemVerilog verification platform that includes support for Verilog, SystemVerilog, SVA, OpenVera, OVM, VMM, UPF and SystemC. MPSim comes integrated with Designer, the most advanced design, SVA and testbench debugger in the industry. Visit us at Booth 479 to learn about companies who have cut down their verification cost by taping out highly complex chips exclusively with MPSim and learn about the new SVA Evaluation Engine (SEE) technology and further advances in Multi-CPU simulation technologies from Axiom.

ACM

Knowledge, Collaboration, & Innovation in Computing

Resources for ACM Members

New and Noteworthy

Communications of the ACM

Fully redesigned and redefined, ***Communications*** is the leading print and online magazine for the computing and information technology fields. Industry leaders use *Communications* as a platform to present and debate various technology implications, public-policies, engineering challenges and market trends. Complimented by a new website featuring advanced browse funcitonality, blogs, archives and much more, *Communications* is truly the world's leading source for advanced computing content and resources.

acmqueue Website

acmqueue is now entirely online offering expanded content, increased frequency and more direct engagement with experts. Guided and written by distinguished and widely known practicing professionals, the expanded acmqueue offers features such as: ***planet queue*** blogs by authors who "unlock" important content from the ACM Digital Library and provide commentary; videos; downloadable audio; CTO Roundtable discussions; plus unique Case Studies.

ACM Online Books and Courses

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The ACM online books program includes **full access to 600 online books** from Safari® Books Online (professional members only), and **500 online books** from Books24x7®. The ACM online course program features **full access to 3,200 online course titles** in multiple languages and 1,000 virtual labs. These courses are open to ACM Professional and Student Members on a wide range of technical and business subjects.

Additional Resources

ACM Local Chapters
www.acm.org/chapters

ACM Conferences
www.acm.org/conferences

ACM Digital Library
www.acm.org/dl

ACM Professional Development
www.acm.org/pd

ACM Special Interest Groups
www.acm.org/sigs

ACM Publications
www.acm.org/pubs

ACM Advanced Member Grades
http://awards.acm.org

ACM-W
http://women.acm.org

ACM Electronic Services
https://www.myacm.org/dashboard.cfm

Special First Year Introductory Membership Offer: www.acm.org/memberoffer4
Select Priority Code: DC3ACMC

EXHIBITING COMPANIES

BEEcube, Inc.
Fremont, CA
www.beecube.com Booth: 1314

BEEcube provides a High-Speed multiple FPGA prototyping and verification platform. With over 150 BEE systems purchased world-wide, BEEcube will present BEE3 technology targeting:

- Computation/Algorithm prototyping
- SOC/IP RTL verification
- SOC/CPU architecture exploration

BEE3's symmetrical Honeycomb™ architecture, coupled with high-speed Sting I/O™, local monitoring and control with the Nectar OS ™, industry's largest Trace memory, was used in verifying CPUs for Sun, and computer architecture for Microsoft, as well as numerous wireless, networking, consumer electronic and video/audio design validation.

Berkeley Design Automation, Inc.
Santa Clara, CA
www.berkeley-da.com Booth: 1102

Berkeley Design Automation, Inc. is the recognized leader in advanced analog, mixed-signal, and RF verification. Its Analog FastSPICE Platform (AFS Platform) combines the accuracy, performance, and capacity needed to verify GHz designs in nanometer-scale silicon. Over seventy companies, including 15 of the world's top 20 semiconductor companies, use the AFS Platform to efficiently verify their nanometer circuits.

BigC
Torrance, CA
www.bigc.com Booth: 350

Dino-Lite Portable Digital Microscopes provide high-quality microscopy video interfacing to PC with clear and steady imaging and 10X–200X magnification. The included "DinoCapture" makes it easy to take snapshots, record videos, manipulate images, and save and e-mail discoveries.

Blue Pearl Software
Santa Clara, CA
www.bluepearlsoftware.com Booth: 1558

Improve design efficiency and reduce your design risk with Indigo RTL Analysis, Cobalt Timing Constraint Generation & Management, and Azure Timing Constraint Validation. These productivity-enhancing tools will help you accurately generate, manage, and validate timing constraints as well as find and debug serious RTL and timing constraint errors early in the design flow. Automatic Clock Recognition makes setup easy. Close timing quickly, improve QoR, reduce design risk, and dramatically decrease your overall cost of design by implementing Blue Pearl Software into your flow.

Bluespec, Inc.
Waltham, MA
www.bluespec.com Booth: 1476

Bluespec is the Synthesizable Modeling Company. With Bluespec, models and testbenches can be synthesized along with legacy IP to employ emulation much earlier for modeling, verification and early software development. Bluespec makes emulation much easier, more affordable, and deployable from concept to volume silicon. Bluespec provides a synthesizable modeling kit and emulation infrastructure, all powered by the only general-purpose, high-level synthesis toolset for any use model (models, testbenches, production IP) and design type (datapath, control, interconnect).

Breker Verification Systems
Austin, TX
www.brekersystems.com Booth: 1121

Breker's Trek™ Scenario Modeling for Advanced Testbench Automation technology for SoC Verification provides functional verification engineers with an automated solution for generating input stimulus, checking output results and measuring scenario coverage. Trek, a proven technology, demonstrates a 10X reduction in test-bench development and 3X improvement in simulation throughput, freeing up resources needed to meet today's aggressive design goals. Architected to run in your current verification environment, this technology also provides powerful graphical visualization and analysis of your design's verification space.

Cadence Design Systems, Inc.
San Jose, CA Platinum Exhibitors
www.cadence.com Booth: 1334

Cadence is the global leader in software, hardware, and services that is driving the transformation of the EDA industry. The Cadence vision for this transformation is called EDA360, because it embraces the entire spectrum of the design process and focuses on end-product profitability. This application-driven approach for creating, integrating, and optimizing designs helps customers realize silicon chips, system-on-chip devices, and complete systems at lower costs and with higher quality. Cadence is headquartered in San Jose, California, with sales offices, design centers, and research labs around the world to serve the global electronics industry.

Calypto Design Systems
Santa Clara, CA
www.calypto.com Booth: 286

Attention RTL designers! Visit booth #286 to see how Calypto's PowerPro CG (for Clock Gating) and PowerPro MG (for Memory Gating) can automatically reduce power by over 60% in your SoC design. For those of you in the ESL space, Calypto's SLEC product family comprehensively verifies RTL designs generated by the industry's leading high-level synthesis tools. Calypto empowers SoC and systems designers to develop the highest quality, lowest power electronic systems through its unique power optimization and functional verification tools.

Cambridge Analog Technologies
Bedford, MA
www.cambridgeanalog.com Booth: 1511

Cambridge Analog Technologies, Inc. (CAT) is a provider of leading edge ultra-low power analog circuits including ADC and PLL catering to SoCs built for a wide array of applications such as wireline, wireless, medical, automotive areas, displays, imaging and embedded control. CAT's precision ADC consume 5x-15x lower power relative to competition, and CAT's all-digital integer and fractional-N PLL serve both general purpose and ultra-high performance applications below 1ps jitter. CAT offers world-class support for its clients and partners.

The Power of Calypto's **Sequential Analysis Technology** will change the way you think about RTL power optimization and functional verification.

PowerPro® CG

Reduces Power by up to 60%

PowerPro CG is an automated RTL power optimization tool that dramatically reduces power through sequential clock-gating with no impact to timing or area.

PowerPro® MG

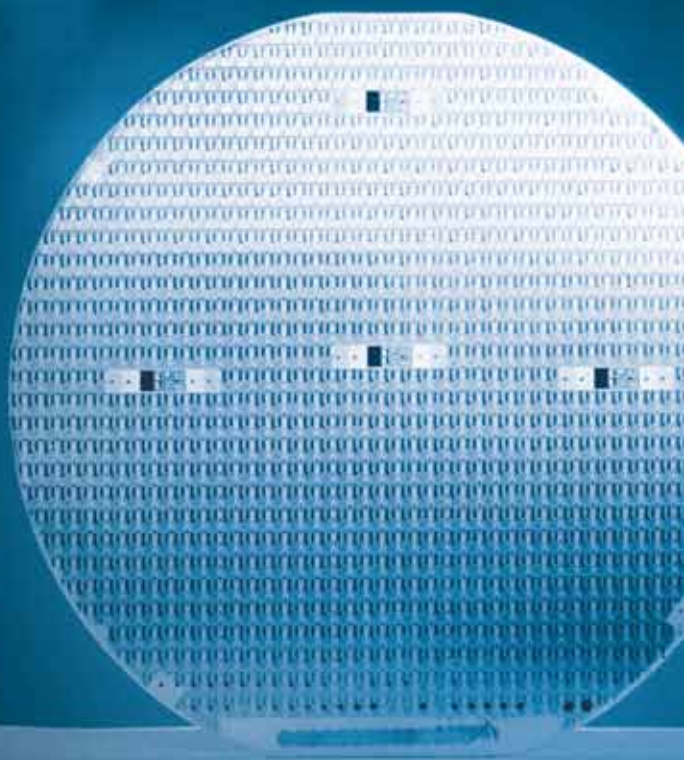
Reduces SoC Memory Power

PowerPro MG automatically reduces SoC memory power in an RTL design by introducing memory gating logic which dramatically reduces both dynamic and leakage memory power.

PowerPro® Analyzer

Provides Full Graphical Visualization

PowerPro Analyzer is a graphical visualization tool that provides designers with a complete understanding of the optimizations generated by PowerPro CG and PowerPro MG. PowerPro Analyzer enables Calypto's PowerAdviser Flow, a power regression flow that facilitates a systematic approach to manually optimizing RTL code during design creation to achieve the lowest power design possible.



SLEC®

Finds Bugs that Other Tools Miss

SLEC is a formal, functional verification solution based on Calypto's unique Sequential Analysis Technology. SLEC comprehensively verifies RTL blocks created manually or generated by High-Level Synthesis (HLS) tools.

CALYPTO®

Empowering the *next* level of design | Visit us at Booth No.286

calypto.com

EXHIBITING COMPANIES

CAST, Inc.
Woodcliff Lake, NJ
www.cast-inc.com Booth: 752
Hundreds of customers trust CAST IP in their FPGA and ASIC systems. With 16 years of development and support experience and a 100-core portfolio, we can help you choose the right IP and provide the deliverables and help you need to succeed with it. Our products include the fastest and smallest 8051s, highest-quality video and image compression cores, solid-state memory controllers, interfaces, peripherals, encryption, AMBA platforms, and reference designs. It's all IP THAT WORKS; stop by to learn more.

ChipEstimate.com
San Jose, CA
www.ChipEstimate.com Booth: 521
All within one site, users can explore an extensive catalog of semiconductor IP and then download the InCyte Chip Estimator tool to predict the die size, power, leakage, performance and cost of their next chip. Visit the ChipEstimate.com booth where you can learn about the latest in semiconductor IP from dozens of IP suppliers on the IP Talks! stage. Join us for hands-on demonstrations and learn how to estimate your next chip's size, power and cost -- in just seconds.

ChipVision AG
Oldenburg, Germany
www.chipvision.com Booth: 1401
ChipVision Design Systems helps semiconductor developers significantly reduce power consumption at the system level. Its award-winning, patented PowerOpt™ solution enables designers to accurately analyze power consumption at the system level and automatically optimize for low power while synthesizing ANSI C++ and SystemC code into Verilog RTL designs, achieving power savings of up to 75 percent compared to RTL designed by hand. The company's solutions are based on open industry standards such as ANSI C++, SystemC, UPF and CPF.

Ciranova, Inc.
Santa Clara, CA
www.ciranova.com Booth: 501
Come see how Ciranova Helix can help circuit designers complete layout for parasitic extraction within minutes or hours, and cut 50% or more from the time required for analog layout. Ciranova provides large productivity improvements in RF, analog and mixed-signal IC physical design. Complementary to existing design flows, Ciranova technology dramatically reduces the time and effort needed to develop device-level layout at both the circuit and PDK levels. Ciranova supports the Si2 OpenAccess database.

CISC Semiconductor Design+Consulting GmbH
Klagenfurt, Austria
www.cisc.at Booth: 1404
CISC Semiconductor is a design and consulting company for industries developing embedded microelectronic systems with extremely short Time-To-Market cycles. Our competences include System design, simulation, verification and optimization of heterogeneous embedded microelectronic systems. The 3rd generation of CISC tool "System Architect Designer" (SyAD®) is a fully featured simulation based verification environment supporting Multi-HDL Modeling, automatic test bench generation, Black and White Box Verification, IP-Xact Library integration, User Access Management within an easy to use Co-Simulation Framework for all major simulators.

ClioSoft, Inc.
Fremont, CA
www.cliosoft.com Booth: 1329
ClioSoft is the premier developer of hardware configuration management (HCM) solutions. The company's SOS design data collaboration platform is built from the ground up to handle the requirements of hardware design flows. The SOS platform gives design teams the freedom and flexibility to choose the way they work, share and collaborate, enabling efficient management of design data from concept through tape-out and improving global team productivity. Custom engineered adaptors seamlessly integrate SOS with leading design flows - Cadence's Virtuoso® AMS and Custom IC Design, Synopsys' Galaxy Custom Designer, Mentor's ICstudio, and SpringSoft's Laker™ Custom Layout Automation System. ClioSoft's innovative Universal DM Adaptor technology "future proofs" data management needs by ensuring that data from any flow can be meaningfully managed.

CLK Design Automation, Inc.
Littleton, MA
www.clkda.com Booth: 373
CLK Design Automation is the technology leader in high accuracy timing solutions for nanometer semiconductor designs with Amber Path FX™; fast SPICE based path timing solution with full statistical analysis for use with PrimeTime™. Amber Path FX uses transistor level modeling to deliver SPICE accurate delay and statistical timing analysis, 100,000x faster than traditional Monte Carlo SPICE. Amber Path FX complements PrimeTime™ and PrimeTime SI™. Amber Path FX was developed in partnership with TSMC for use with its 40nm libraries.

CMP
Grenoble Cedex, France
www.cmp.imag.fr Booth: 644
CMP is a manufacturing broker for ICs and MEMS, for prototyping and low volume production. Since 1981, more than 1000 Institutions from 70 countries have been served. Integrated Circuits are available on CMOS down to 40 nm, SiGe BiCMOS (down to .35 µ), CMOS-Opto (.35 µ). ARM IP cores are available on .12 µ and 65 nm CMOS. MEMS are available on various processes: front-side bulk micromachining, ASIMPS from MEMSCAP, MUMPS from MEMSCAP, SUMMiT from SANDIA. Design kits for most IC CAD tools and Engineering kits for MEMS are available.

CoFluent Design
Le Chesnay, France
www.cofluentdesign.com Booth: 1415
CoFluent Design provides Eclipse-based system-level modeling and simulation tools for executing use cases and predicting performance of embedded systems and chips. CoFluent Studio allows designers to model real-time embedded applications and use cases, simulate their execution on multiprocessor/multicore platforms, and obtain power and performance data. Models are captured in graphical diagrams using standard UML or CoFluent domain-specific language. Algorithms can be captured in ANSI C/C++ or with MATLAB. Models are translated into TLM SystemC code for host-based simulation. The generated SystemC can be reused as functional or test model in virtual platform environments.

DAC Pavilion

Booth 694

Monday, June 14 - Wednesday, June 16

EXHIBITING COMPANIES

Compaan Design BV
Amsterdam, The Netherlands
www.compaandesign.com Booth: 368

Compaan Design develops technology for hotspot parallelization of legacy/certified ISO C applications and offers innovative products that reliably compile to state-of-the-art silicon with billions of transistors like x86 multicore, MPSoC, and FPGA. The Compaan Design workflow guides step-by-step parallelization towards improved energy efficiency and computational throughput. Parallelism is exploited for streaming data and increased architecture utilization. Exact dataflow analysis guarantees correctness and robustness of application execution. Code generation supports heterogeneous MPSoC architectures with custom processors, DSPs, FPGAs and IP blocks.

Concept Engineering GmbH
Freiburg, Germany
www.concept.de Booth: 513

Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers and IC and FPGA designers. Their products include, NIview™ Widgets - a family of schematic generation engines for EDA tool developers, SpiceVision® PRO - a customizable debugger for SPICE and DSPF designs, RTLVision® PRO - a graphical debugger for SystemVerilog, Verilog and VHDL designs, GateVision® PRO - a customizable debugger for Verilog designs. SGvision™ PRO - a mixed-mode debugger.

Coupling Wave Solutions
Austin, TX
www.cwseda.com Booth: 1219

Coupling Wave Solutions® (CWS) WaveIntegrity platform targets analysis and resolution of parasitic coupling between digital cores and analog or RF blocks and helps successful integration of Mixed-Signal SOCs and SIPs. WaveIntegrity offers full system noise calculations from initial system-level definitions to layout level. WaveIntegrity automatically analyzes the complete system to predict electrical aggression generated by all components, propagation through a combination of interconnects, silicon substrate and package parasitics and the impact on sensitive analog/RF blocks. The technology predicts noise budgets, supports designs having multiple power domains and integrates seamlessly into any customer flows.

CST of America, Inc.
Framingham, MA
www.cst.com Booth: 1462

CST develops and markets software for the simulation of electromagnetic fields in all frequency bands. Its products allow you to characterize, design and optimize electromagnetic devices before going into the lab or measurement chamber. This can help save substantial costs especially for new or cutting edge products, reduce design risk and improve overall performance and profitability. Customers operate in industries as diverse as Telecommunications, Defense, Automotive, and Medical Equipment, and include market leaders such as IBM, Intel, Mitsubishi, and Siemens.

Cybereda Corp.
San Jose, CA
www.cybereda.com Booth: 164

Come discover PCSIM — the new generation transistor-level simulator for analog designers, and ADDS — a breakthrough analog circuit debugger. With its unique CyberParallel™ technology, PCSIM delivers 10X better runtimes versus popular commercial SPICE simulators with no compromise in precision of results. ADDS attacks the productivity gap in analog circuit debug and delivers a 10X reduction in time spent bug killing. With Cybereda ADDS and PCSIM you will find the right answers in minutes not days.

DAC Pavilion
Louisville, CO
www.dac.com Booth: 694

Open to all attendees, the DAC Pavilion, sponsored by GLOBALFOUNDRIES, brings the technical conference to the exhibit floor with a wide variety of panels and presentations featuring seventeen technical, business and strategy discussions. Panels include discussions on Analog, FPGA, System-Level Design, IP, Multicore, SOC, SPICE, and Verification. In addition, the Pavilion offers sessions such as "Everyone Loves a Teardown," the EDA Heritage Series Session and the popular Gary Smith on EDA and Hogan's Heroes sessions. See pages 51-54, visit DAC.com or stop by booth 694 for a complete schedule.

Dassault Systemes Americas Corp.
Lowell, MA
www.3ds.com Booth: 1370

A world leader in 3D and Product Lifecycle Management (PLM) software and services, Dassault Systèmes (DS) brings value to 115,000 customers in 80 countries. The DS portfolio includes CATIA for virtual design, SolidWorks for 3D mechanical design, DELMIA for virtual production, SIMULIA for virtual testing, ENOVIA for global collaboration and 3DVIA for online 3D experiences. The ENOVIA Synchronicity DesignSync solutions uniquely address a rapidly emerging use for PLM by helping customers connect their electronic design environments directly to the extended enterprise. This enables globally dispersed design teams to collaborate in real time, reducing design and development costs, leveraging design expertise, improving quality and accelerating time to market. Learn more at http://www.3ds.com/enovia/semiconductor.

DATE 2011
Edinburgh, United Kingdom
www.date-conference.com Booth: 845

DATE is the complete event for the European electronic system and test community. A world-leading conference and exhibition, DATE unites 2000 professionals with some 60 exhibiting companies, cutting-edge R & D, industrial designers and technical managers from around the world. As per previous editions the DATE 2011 conference will feature two special days. The technical paper submission is 5 September 2010. Please visit our website for further details.

At Dassault Systèmes,
Innovation is a Core Value

Innovation is at the core of what Semiconductor and High-Tech Electronics companies do. Understanding how to incorporate new, innovative technologies into the next 'must have' products customers are demanding – and validate those products without delaying rapid launch schedules is critical to your success!

Semiconductor and High-Tech Electronics companies need effective solutions to:

- rapidly evaluate design performance
- foster collaboration across multiple design teams
- access most current data on product parts and IP
- leverage the know-how of experts using advanced EDA tools and methodologies
- ensure compliancy with stringent government regulations

The traditional process of producing prototype parts followed by physical testing is time consuming. Semiconductor and High-Tech companies need a way to quickly and accurately evaluate and improve product performance during the design process while reducing the risk of failed prototypes or worse, failure in the field.

That's why, to stay competitive, more than 25 leading global consumer electronics manufacturers and more than 100 semiconductor organizations, including 17 of the top 20 semiconductor companies, are using solutions from Dassault Systèmes, including **ENOVIA Synchronicity** for collaborative design management and **SIMULIA Abaqus FEA** software for realistic simulation.

Advanced PLM (Product Life Cycle Management) solutions from Dassault Systèmes enable companies to manage change and streamline their processes more effectively – from idea generation to concept validation, including product portfolio management visibility, collaborative IP development, sourcing, production, change management and sign-off.

Meet DS PLM experts & learn about our technology at Booth # 1370 in the Exhibit Hall!

DASSAULT SYSTEMES

EXHIBITING COMPANIES

Denali Software, Inc.
Sunnyvale, CA
Gold Exhibitors
www.denali.com
Booth: 1183
Denali Software is a world-leading provider of electronic design automation (EDA) tools, intellectual property (IP), software and design platforms for system-on-chip (SoC) design and verification. We deliver the industry's most widely-used solutions for deploying PCI Express, USB, NAND Flash and DDR SDRAM subsystems in electronic designs. Developers use Denali's EDA, IP products and services to simplify design, reduce risk, and accelerate time-to-market for their complex SoC designs. Incorporated in 1996, Denali is headquartered in Sunnyvale, California and serves the global electronics industry with direct sales and support offices in North America, Europe, Japan and Asia.

Design and Reuse
Grenoble Cedex 1, France
www.design-reuse.com
Booth: 1150
Founded in 1997, D&R became the worldwide leader as a web and a B2B portal in the IP/SoC field with its 70,000 Absolute Unique Visitors / Month (source: Google Analytics), 15,000 daily updated IP/SOC products descriptions, its News broadcast to 35,000 subscribers… Based on 13 years experience, D&R sells a Java/XML multi application, configurable enterprise platform offering the most innovative and straightforward solution for your hottest needs such as Web Product cataloguing, intranet Design Reuse Platform, External suppliers management…

Dini Group
La Jolla, CA
www.dinigroup.com
Booth: 778
New products featuring Xilinx Virtex-6 technology will be on display, including the new DN2076k10 with 6 LX760 devices. Dini will also display the world's largest ASIC Prototyping Platform, the DN7020k10 with 20 Altera Stratix-4 devices providing more than 100 million ASIC gates. Founded in 1995, the Dini Group has supplied over 5 billion ASIC gates and driven prices below 1/4 Cent/ASIC gate.

DOCEA Power
Moirans, France
www.doceapower.com
Booth: 1458
DOCEA Power develops and commercializes a new generation of methodology and ESL tools for enabling faster and more reliable power and thermal modelling at system level. DOCEA Solution based on the ACEplorer® platform is a consistent approach for executing architecture exploration and optimizing power and thermal behaviour of electronic systems at an early stage of the project. Founded in 2006 the private company DOCEA Power is based in the Grenoble area, France.

Dorado Design Automation, Inc.
Hsinchu, Taiwan
www.dorado-da.com
Booth: 680
Dorado expands the scope of ECO to be "All the incremental jobs to be done in the ECO phase", and commit to provide solutions for all ECO issues. Dorado's Tweaker family covers all possible incremental jobs such as Functional ECO, Timing ECO, Metal ECO, Power ECO, and the interesting pre-route ECO for SI prevention. Tweaker family is developed with ECO specific architecture and algorithm. It supports 40nm and below.

Duolog Technologies Ltd.
Sandyford, Dublin, Ireland
www.duolog.com
Booth: 568
Duolog introduces Socrates – the hub for IP integration. Socrates replaces ad-hoc scripted solutions with a centralized, standardized, synchronized IP integration platform. The Socrates tools incorporate IP packaging, register management, rules-based system assembly and I/O fabric creation. Socrates auto-generates multiple design views from a standardized, centralized data source so that all teams are synchronized at all times, guaranteeing higher quality designs, more predictable schedules and fewer bugs. The Socrates tools fully support IP-XACT and run on Windows or Linux platforms.

E-System Design
Johns Creek, GA
www.e-systemdesign.com
Booth: 261
E-System Design E-System Design was founded in March 2009 by industry leading EDA, Semiconductor, and Signal and Power Integrity experts to provide EDA software focused on enabling System Integrity through Signal and Power Co-simulation of complex, high speed and highly integrated IC packages, SIPs, printed circuit boards, and systems. E-System Design's initial product, "Sphinx" is a "Best in Class" Signal and Power Co-simulator capable of accurately simulating critical paths through complete designs for evaluation and signoff of new designs for production release.

EDA Cafe-IB Systems
Campbell, CA
www.edacafe.com
Booth: 1015
Thousands of IC, and system designers visit EDACafé.com to learn about the latest company news and research the latest design tools and services. As the #1 EDA portal it attracts more than 75,000 unique visitors each month and leverages TechJobsCafe.com to bring you targeted job opportunities. EDACafé reaches out to more than 30,000+ EDA professionals with its daily CaféNews. EDACafe will be doing video interviews of industry executives at its DAC booth. Please visit to hear all the conference buzz.

EDXACT SA
Voiron, France
www.edxact.com
Booth: 1170
EDXACT provides independent and controllable parasitic management technologies, necessary in today's demanding designs, where the impact of the parasitics on the design performance is getting more important than that of the designed transistors. EDXACT's tool solutions can easily be integrated into the major EDA flows, providing important gains in productivity and quality. The tools are available in batch mode, but GUIs are also available for all major flows. JIVARO reduces the burden of back annotated RC(LK) parasitics on transistor level simulators. The flexibility of JIVARO, the possibility of selectively applying different reduction schemes, combined with the fact that the user has control over the accuracy, make JIVARO a tool that has been chosen by leading edge IDMs and fabless semiconductor companies. COMANCHE analyzes the interconnect parasitics of a design extremely quickly. The main applications of COMANCHE in production are today ESD validation, Latchup verification, extraction tool validation, pre-simulation verification and design exploration and debugging.

EDACafé

As the #1 EDA portal, EDACafé.com attracts more than 75,000 unique visitors each month and leverages TechJobsCafé.com to bring you targeted job opportunities. EDACafé.com reaches out to more than 30,000+ EDA professionals with its daily newsletter. Sign up for our daily newsletter at EDACafé.com.

www.EDACafé.com

EXHIBITING COMPANIES

Entasys Inc.
Seoul, Republic of Korea
www.entasys.com Booth: 351

Entasys provides an Electronic System Level (ESL) Silicon Virtual Prototyping (SVP) solution to fill the technology gap between ESL and IC implementation designers. To predict the design problems of IC implementation the company delivers feasibility analysis features as follows: power and area estimation, flexible IO pad configuration including optimization of the number and location of power pad, initial floorplanning, power network prototyping and routing congestion analysis. Entasys products enable you to achieve high performance and design time reduction with early design planning solution.

Enterpoint Ltd.
Worcestershire, United Kingdom
www.enterpoint.co.uk Booth: 1402

Specialists in FPGA boards, IP and services Enterpoint offers innovative ASIC development and High Performance Computing Platforms. The Broaddown family of products offer high end FPGA solutions in PCI and PCIe formats and target both ASIC and HPC markets. Our Merrick family of products offers highly cost effective HPC solutions in a compact and power efficient package. Our solution range is supplemented a wide range of I/O modules and semi / full custom design of boards and IP.

EVE-USA, Inc.
San Jose, CA
www.eve-team.com Booth: 510

EVE's ZeBu suite of hardware-assisted verification solutions, including its 6th generation ZeBu-Server, provides the industry's leading HW-SW Co-verification platform, highest performance and lowest cost-of-ownership. Hardware designers and embedded software developers can shorten time to revenue for complex chips and electronic systems design, leveraging ZeBu throughout the design cycle. EVE provides broad support with interfaces to Verilog, SystemVerilog and VHDL-based simulators, Electronic-System Level (ESL) tools, and target hardware systems across the range of computer, consumer, networking, communications, and automotive industries.

Exhibitor Forum
Louisville, CO
www.dac.com Booth: 1562

The Exhibitor Forum provides a theater on the exhibit floor where exhibitors present focused, practical technical content to attendees. Each session is devoted entirely to a specific domain (e.g., verification or system-level design) and consists of presentations from two to three companies. The Exhibitor Forum provides exhibitors and attendees with a great way to network, and is yet another way that DAC delivers practical "how-to" information and introduces new technologies on the exhibit floor.

ExpertIO, Inc.
www.expertio.com Booth: 1416

ExpertIO, Inc. is a world-class provider of Verification IP and Design / Verification Services. Our goal is to deliver the highest quality and easiest to use Verification IP on the market. Founded in 2002, ExpertIO has been entrusted by clients around the world when time to market matters. Current Verification IP products include:

- PCI Express
- Ethernet (10Mb to 100Gb)
- SATA
- SAS
- Fibre Channel

Our products are designed and backed by our all senior engineering team of protocol verification experts. Let ExpertIO help you achieve 1st pass success and improve your time to market! Phone: 408-217-1901.

Extension Media LLC
San Francisco, CA
www.extensionmedia.com Booth: 1554

Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. Also, be sure and visit www.http://eecatalog.com/ for valuable information about all of Extension Media's outstanding technology resources.

Extreme DA
Santa Clara, CA
www.extreme-da.com Booth: 556

Wondering which Timing tool to use for design closure? Come discover GoldTime, the 'No Compromise' timing engine that delivers 250M cell instance capacity, sign-off accuracy and the fastest runtimes for SI and statistical analysis. Why use an unverified timer, when GoldTime has shown proven silicon and dozens of tapeout for fabless companies. Learn how GoldTime POCV delivers lightweight statistical analysis better than AOCV. Whether verifying timing at 65nm or yield at 32nm, GoldTime delivers the right answers you need – FAST!

FishTail Design Automation, Inc.
Lake Oswego, OR
www.fishtail-da.com Booth: 186

FishTail Design Automation offers a unique approach to improving chip implementation by automatically generating, merging, promoting and verifying golden timing constraints early in the design cycle. FishTail's products allow designers to drive chip-implementation with complete constraints that are formally proven to be correct and to then manage these constraints as chip-implementation progresses. The result is a shorter chip-implementation schedule with much fewer back-end timing closure iterations. Also, by formally proving the correctness of design constraints you eliminate the risk of silicon failure resulting from incorrect timing exceptions.

The Network For Advanced IC Designers

Magazines

In-depth coverage of all the technical challenges and implementation options that engineers face in the development and manufacturing of today's complex integrated circuits (IC)

Resource Catalogs

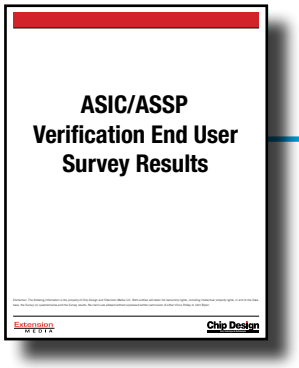
Locate vendors and products including IP, ASIC's, FPGA's, SoC, EDA tools, design services and more

Websites

Online source for the latest tools, technologies and methodologies to better navigate the challenges that face modern IC design environments

Email Newsletters

Email newsletters and online periodicals with news, commentary and analysis



Market Research

Valuable market intelligence on Chip Design trends

www.chipdesignmag.com

EXHIBITING COMPANIES

Forte Design Systems
San Jose, CA
www.forteds.com Booth: 750
Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction and improve design results. Its innovative synthesis technologies and intellectual property offerings allow design teams creating complex electronic chips and systems to reduce their overall design and verification time. More than half of the top 20 worldwide semiconductor companies use Forte's products in production today for ASIC, SoC and FPGA design. Forte is headquartered in San Jose, Calif., with additional offices in England, Japan, Korea, and the United States.

Gary Stringham & Associates, LLC
Eagle, ID
www.garystringham.com Booth: 1405
Struggling to integrate firmware (embedded software) with hardware? Spending millions of dollars and months in delays to respin a chip? Trying to diagnose and resolve hardware/firmware interaction problems? Principles and practices developed by Gary Stringham & Associates will eliminate or mitigate defects, respins, and delays in ASICs, ASSPs, SoCs, and FPGAs regardless of the EDA tool chain in use. GS&A provides consulting and training to engineers to improve productivity, quality, and time-to-market. Come see Gary's book, Hardware/Firmware Interface Design.

GateRocket, Inc.
Bedford, MA
www.gaterocket.com Booth: 1319
GateRocket is the only company specifically addressing the increasing challenge of verifying and debugging complex FPGAs. Its unique Device Native® approach verifies the design using the targeted FPGA device in its RocketDrive® verification system, saving weeks in the debug lab, eliminating many costly synthesis-place-route iterations, and reducing FPGA bring-up time by 50% or more. The RocketDrive and its accompanying software debug tool, RocketVision®, turn an existing HDL simulator into a powerful and efficient FPGA debugging system that provides unprecedented visibility into designs and dramatically reduce the 'vicious cycles' of traditional FPGA design approaches.

GiDEL
Santa Clara, CA
www.gidel.com Booths: 908, 912
GiDEL, the first company to provide third-generation ASIC Prototyping systems in the market, will be showcasing its new generation of the PROC_SoC Verification System. The PROC_SoC family is designed to debug and verify SoC designs of diverse design styles. The new generation has quadrupled the capacity of the system by incorporating Altera's new Stratix IV 820E, the world's largest and fastest 40nm FPGA available today. The PROC_SoC system incorporates advanced software tools, enabling easy HW/SW co-development and powerful debug features, and is packaged in two types of chassis each providing a high degree of flexibility and mobility. For more information, contact GiDEL in North America at 408-969-0389.

GLOBALFOUNDRIES
Sunnyvale, CA
Gold Exhibitors
www.globalfoundries.com Booths: 275, 370, 374, 574
GLOBALFOUNDRIES is the world's first full-service semiconductor foundry with a truly global manufacturing and technology footprint. With a unique combination of advanced technology, manufacturing excellence, and global operations, the company is able to offer best-in-class foundry services from mainstream to the leading edge. GLOBALFOUNDRIES is headquartered in Silicon Valley with manufacturing operations in Singapore, Germany, and a new leading-edge fab under construction in Saratoga County, New York.

Gradient Design Automation
Santa Clara, CA
www.gradient-da.com Booth: 686
Gradient can help you design higher quality and more reliable chips. Our software simulates the temperature inside a chip or 3D-IC at very fine granularity. The products fit into the standard EDA flows, and produce temperature profiles that help reveal thermally-induced circuit failures and performance degradations during the design process, before tapeout, so that corrective actions can be taken. By adding temperature-awareness to the design ecosystem, Gradient improves electrical simulation accuracy and reveals opportunities to neutralize the temperature effects.

Grid Simulation Technology, Inc.
Morgan Hill, CA
www.gridsimtech.com Booth: 1262
GRID Simulation Technology, Inc. is a Silicon Valley-based Electronic Design Automation (EDA) company dedicated to solving the world's largest and most complex electronics problems at true SPICE-accuracy through its revolutionary new analysis technology. The company's flagship products, NanoRAIL™ and SimCHECK™, provide analysis of IC power grid problems including IR voltage drop and electro-migration (EM), and the qualification of complex power network analysis results. The company is a privately held California Corporation headquartered at the southern extent of Silicon Valley in Morgan Hill, CA and with offices located in: Los Angeles, CA; East Fishkill, NY; and Tokyo, Japan.

Helic, Inc.
San Francisco, CA
www.helic.com Booth: 1450
Helic, Inc. develops disruptive EDA technology for RFIC and System-in-Package design. We provide our customers with a service model combining EDA tools, IP and services, enabling first-pass silicon while greatly reducing the development cycles of integrated wireless transceiver products. VeloceRF™ is our leading EDA tool for integrated inductor synthesis, modeling, and verification. Helic's products have been adopted by many renowned semiconductor companies worldwide, with over 500 designers using our tools.

EXHIBITOR FORUM

Hall B
Booth 1562

The Exhibitor Forum features cutting edge solutions to today's most extreme design challenges. Exhibitor Forum presentations were reviewed and selected based upon their educational and technical value.

See pages 55-56 for details...

Amiq Consulting S.R.L.
Apache Design Solutions, Inc.
CoWare, Inc.
Cadence Design Systems, Inc.
EVE-USA, Inc.
Extreme DA
FishTail Design Automation, Inc.
GateRocket, Inc.
IC Mask Design Ltd.
Tanner EDA
Real Intent, Inc.
Synfora, Inc.
Synopsys, Inc.

EXHIBITING COMPANIES

Hewlett-Packard Co.
Houston, TX
www.hp.com
Booth: 555
HP is an industry leader in EDA high-performance computing, scalable computing infrastructure and storage solutions. A broad choice of platforms, services, operation systems and applications is available on HP workstations, servers, blades and clusters. HP partners with the leading EDA software providers to ensure customers get the highest performance for design productivity and time to market. Please visit HP at DAC 2019 to discuss your EDA computing and storage requirements. Also visit HP at www.hp.com/go/eda.

HiPEAC
Ghent, Belgium
www.hipeac.net
Booth: 476
HiPEAC (High-Performance and Embedded Architecture and Compilation) is a Network of Excellence (NoE) that gathers 150+ leading European academic and industrial computing system researchers in one virtual centre of excellence. Its purpose is to coordinate their research, improve their mobility, and increase their visibility. HiPEAC's mission is to steer and increase the European research in the area of high-performance and embedded computing systems as well as stimulate cooperation between academia and industry, computer architects and tool builders.

IBM Corp.
Armonk, NY
www.ibm.com
Booth: 1305
IBM is a leading provider of information technology hardware, software, and services. Based on extensive in-house semiconductor research and development as well as numerous successful engagements with leading clients around the world, IBM Rational, Tivoli, Systems and Technology Group, and Global Business Services provide integrated solutions that span semiconductor design, verification, and manufacturing.

IC Manage, Inc.
Los Gatos, CA
www.icmanage.com
Booth: 550
IC Manage provides a high performance, scalable, reliable design management system, for managing IC design data across global design teams. IC Manage Global Design Platform (GDP) is a comprehensive set of tools and configurable workflows to improve product quality, designer productivity, team collaboration, bug tracking, and IP reuse and management of derivative designs. GDP also includes built-in IT capabilities such as hot backup, high availability, and disaster recovery for 24x7 enterprise availability.

ICDC Partner Pavilion & Stage
Louisville, CO
www.dac.com
Booth: 1710
The IC Design Central Partner Pavilion brings together vendors supplying products and services that address many of the critical design functions necessary to produce working silicon on time and on budget. Companies from all areas of the design and product development process—EDA, Foundry, IP, Design Services, Assembly/Package, Test, and System Interconnect—must cooperate to offer integrated front-to-back solutions that ensure first-time-successful silicon and predictable time-to-market. Visit the IC Design Central Partner Pavilion and find design flows and solutions needed to create today's challenging designs.

IMEC - Europractice
Leuven, Belgium
www.imec.be
Booth: 372
The EUROPRACTICE IC service offers low cost and easy access to ASIC prototyping and small volume fabrication in industrial CMOS processes from 0.8µ to 40nm at well-known foundries (ONSemi, austriamicrosystems, IHP, LFoundry, TSMC, UMC, Faraday). A total manufacturing flow is offered (standard cell library, design kit access/deep submicron RTL-to-layout/prototyping/volume fabrication/qualification/assembly/test).

Imera Systems, Inc.
San Jose, CA
www.imera.com
Booth: 185
Imera offers next-generation virtual network infrastructure and secure cloud solutions to enable critical business processes. Imera solutions secure computing resources within private and public clouds and connect computers, design data, and people across eco-system. Design teams can instantly protect servers and design data on premise for EDA vendors to perform remote debug without IP leaks. Imera also enables design houses to leverage public cloud and meet peak computing requirement by protecting applications and data in multi-tenancy environment.

Infotech Enterprises
San Jose, CA
www.infotech-enterprises.com
Booth: 461
Infotech Enterprises founded in 1991, is an 8,000 people company. HiTech Business Unit (including the acquisition of Time to Market) provides engineering services for RTL Design & Verification, DFT, Synthesis/Timing, Physical Design & Verification, Custom/Analog Layout, Embedded Software (board support package, middleware customization, OS porting, device driver development, connectivity software development and multimedia component (audio/video) integration) and FPGA/Board design with 12 year impeccable track record of "first pass success" on over 200 design projects across various nodes up to 40nm.

iNoCs
Lausanne, Switzerland
www.inocs.com
Booth: 1510
iNoCs is the supplier of next-generation on-chip interconnection technology for System-on-Chips, multicore products and FPGAs. Founded by a pioneering team in Networks-on-Chips, iNoCs develops NoC design tools and NoC RTL IP libraries to tackle on-chip communication demands quickly, efficiently and in a plug&play fashion. Advantages include much faster timing closure; improved product time-to-market; reduced design effort; scalable performance; easy integration with existing EDA flows.

Interra Systems, Inc.
Cupertino, CA
www.interrasystems.com
Booth: 244
Interra Systems is a broad-based software products and services provider in Design Automation and Digital Media industries. Interra Design Automation solutions are led by Memory development system (MC2), standards-compliant EDA building blocks (EDA Objects) and HDL coverage test suites. EDA Objects from Interra have been in production use for over fifteen years. They include Verilog/VHDL parsers, elaborator, and synthesis engine. Products and Services from Interra are differentiated by deep engineering knowhow and proven track record of supporting customers.

EDA and IC

IP | Design Services | Foundry | TEST/BIST
Interconnect | Workload Management | and More!

The ICDC Partner Pavilion is a combination of exhibit booths and 30-minute presentations by each participating vendor. The combination of product displays in the exhibits and technical product presentations in the ICDC Theater offers attendees an in-depth look into flows and methodologies from vendors featuring a variety of products and services for the entire design ecosystem.

IC Design Central Partner Pavilion

Hall B Stage #1710

See pages 61-63 for details...

EXHIBITING COMPANIES

Jasper Design Automation, Inc.
Mountain View, CA
www.jasper-da.com Booth: 1337

Jasper Design Automation offers high-value solutions for the design and verification of semiconductors and electronic systems, based on formal technologies. Jasper delivers advanced formal technology, software and services to the global electronics market including consumer, wireless, computing, network, graphics, and other markets. Flagship products JasperGold, JasperCore, and ActiveDesign give customers a competitive advantage by delivering value throughout the design cycle, with targeted ROI effects. Headquartered in Mountain View, California, Jasper is privately held and has offices and distributors worldwide.

Jspeed Design Automation, Inc.
San Jose, CA
www.jspeedda.com Booth: 811

Jspeed Design Automation, Inc. is specialized in routing large-scale flat designs. The company's flagship product, JaguarRoute (JRoute) is a cutting-edge IC router for both standard and custom cell designs with process technology of 65 nm and below. For fully or partially routed designs, JRoute is able to identify and fix violations and optimize the routing results with minimal changes. Our technology can handle flat designs of an almost unlimited size, reduce the wire count up to 50%, via count by 10%, and runtime by 80% (5X for single-core CPU), and is very capable at routing highly congested designs.

JTAG Technologies
Stevensville, MD
www.jtag.com Booth: 254

The JTAG Live product family helps solve hardware debug problems, quickly and easily locating prototype faults. JTAG Live is especially useful for boards that are difficult to access with conventional probing methods such as DMMs, scopes, and analyzers. By means of existing boundary-scan resources on your board, you gain visibility into the status of inaccessible nets and pins. The JTAG Live graphical screen shows you the pin-level details of the boundary-scan ICs on your board.

Laflin Limited
Portland, OR
www.laflinltd.com Booth: 362

Laflin Limited sells/supports EDA tools, IP, and Design Services for leading providers in the electronics industry. Represented at DAC will be: Instigate Design, a design services company based in Armenia, with more than 30 successful customer engagements in U.S./Europe and a staff of ~100 engineers. Expertise lies in:

- Massive parallel algorithms System modeling/simulation
- Hardware-software decomposition/co-design
- SW development/quality-assurance RTL design/verification

HOTSCOPE v7.5.2 from JEDAT(/DNP) will be displaying its enhanced equivalent net trace capability, schematic viewing of SPICE and EDIF netlists, and LEFDEF net connectivity and element viewing.

Legend Design Technology, Inc.
Santa Clara, CA
www.legenddesign.com Booth: 543

Legend Design Technology Inc. provides the following EDA software products.

1. MSIM Accurate Spice Circuit Simulator for
   (a) Analog/RF/Mixed-Signal IC and IP designs
   (b) LCD and OLED designs
   (c) Package and PCB designs
2. Turbo-MSIM Fast Spice Circuit Simulator for
   Large circuit simulation and full-chip verification
3. Semiconductor IP Characterization/Verification Products
   (a) CharFlo-Memory! : Memory Characterization Toolset
   (b) CharFlo-Cell! : Cell Library Characterization Toolset
   (c) Model Diagnoser : Cell Library Model QA and Debugging Toolset

Library Technologies, Inc.
Saratoga, CA
www.libtech.com Booth: 580

Exhibiting ChipTimer, design reoptimization and timing closure tools, improves clock speed by 30-200%, reduces gate-count by ~10% using design-specific library cells derived from existing library, works for all processes. SolutionWare, Cell, IO and Memory Characterization-Modeling for Timing; automatic verification including memories; CellOpt, timing and power Optimizer for cells and simple blocks like adders and multipliers; YieldOpt, statistical process variation analyzer which does away with SSTA and Monte-Carlo; PowerTeam: dynamic gate level power Verilog based simulator using special libraries generated by SolutionWare.

Lynguent, Inc.
Portland, OR
www.lynguent.com Booth: 1550

Lynguent®, Inc. enables innovation by breaking through the traditional barriers in the design and verification of complex analog and mixed-signal (AMS) electronic systems and components. Customers, using Lynguent's productivity tools, are able to rapidly create and validate AMS models; efficiently bridge system and circuit design; and encapsulate the AMS portion of their design so that it can be used in their existing digital simulator. Lynguent also provides expert consulting and modeling services.

Magma Design Automation, Inc.
San Jose, CA
www.magma-da.com Booth: 602

Since 1997, Magma has been shaking up the EDA industry with groundbreaking software that saves time, effort and money while delivering better results. We were the first to integrate synthesis with place and route, the first to integrate analog and digital design, and now we're revolutionizing timing analysis and automating analog design. Visit our booth to learn the latest about the Talus IC implementation, Titan analog/mixed-signal design, Tekton static timing analysis, Quartz physical verification, FineSim circuit simulation and SiliconSmart characterization solutions. We're rockin' your world – again.

InsideChips™

Focused on Semiconductor Innovation and Ventures

Watch the birth of the hottest chip startups on the planet!

VENTURE FED • ORGANICALLY GROWN • FREE RANGE

www.InsideChips.com

EXHIBITING COMPANIES

Magwel NV
Leuven, Belgium
www.magwel.com Booth: 181

Magwel's Power Transistor Modeler simulates large power transistor arrays, ESD structures and power distribution networks to extract 3D resistance, analyze electro-migration problems, IR drops , and electro-thermal problems with 3D accuracy and unprecedented speed. Substrate Noise Analyzer models substrate noise injection (minority and majority carriers), propagation and coupling in large critical layouts. DevEM co-simulates semiconductor active and passive devices together with metal stack. Parasitic Extraction Tool extracts R, L and C on large critical nets.

MathWorks, Inc.
Natick, MA
www.mathworks.com Booth: 534

The MathWorks is the leading developer and supplier of software for technical computing and Model-Based Design. Over 1,000,000 engineers and scientists in more than 100 countries, on all seven continents, use MATLAB® and Simulink®. These products have become fundamental tools for work at the world's most innovative technology companies, government research labs, financial institutions, and at more than 3,500 universities. Employing more than 2,000 people, The MathWorks was founded in 1984 and is headquartered in Natick, Massachusetts, with offices and representatives throughout the world.

Menta
Montpellier Cedex 2, France
www.menta.fr Booth: 816

Menta licenses the world's first pure soft embedded-FPGA IP core for SoC. Menta's revolutionary ultra-compact technology increases embedded-FPGA (eFPGA) application range to new levels. This ultra-compact architecture provides the SoC designer with the post-fabrication flexibility at near ASIC performance. Menta's soft IP easily integrates into SoC as it leverages standard HDL design flow. Furthermore being soft, the IP is technology independent, so can be targeted to any process technology. The architecture of Menta's FPGA is highly customizable. This allows to create domain-specific FPGA giving enormous benefits in terms of Area, Power and Speed.

Mentor Graphics Corp.
Wilsonville, OR
Gold Exhibitors
www.mentor.com Booth: 1383

Mentor Graphics is a technology leader in electronic design automation, providing software and hardware design solutions focused on IC design, place & route, physical verification, functional verification, FPGA/PLD, design-for-test, PCB design and emerging technologies such as ESL, thermal and EMI analysis. Our innovative tools solve demanding design challenges including scalable solutions for functional verification; cutting-edge technology for design-for-manufacturability and mixed-level IC design verification; award-winning test compression technology; embedded software development systems; and market-leading integrated system design solutions.

Mephisto Design Automation
Leuven, Belgium
www.mephisto-da.com Booth: 264

MDA is the provider of M-Design, the leading analog and mixed-signal design platform that supports designers to efficiently specify, investigate, simulate, optimize, verify and document their design intent. A unique, interoperable user-interface combined with advanced scripting capabilities, a toolbox for analysis post-processing, patent-pending multi-level optimization makes this advanced design platform a must-have for smart and creative designers. M-Design supports different design styles and use-models and enables IP reuse.

Methodics LLC
San Francisco, CA
www.methodics-eda.com Booths: 1622

Methodics' tools provide design data management and IP reuse solutions for semiconductor design and development. Our open architecture DM client plug-in to the Cadence design environment allows the latest generation SCM databases (Subversion, Perforce or Clearcase) to centralize all IC project data. Millions of software, firmware and RTL developers already use one of these databases, making VersIC the most extensible, tested and bug free DM solution available today. VersIC also includes "EDA Enabled" tools including Visual Schematic/Layout Diff and Merge tools, Design Review tools and Continuous Integration tools for Mixed-Signal designs.

Micro Magic, Inc.
Sunnyvale, CA
www.micromagic.com Booth: 1249

Micro Magic, Inc. - Chip Solutions Company MMI provides tools and services for high-speed, low-power Systems on Chip. MMI Tools are field proven with hundreds of tapeouts over ten years. DataPath Compiler - DPC - a unique solution for optimizing datapaths for high-speed and low-power. New DPC features include Verilog-only and gate Auto-sizing. MAX-3D - the only layout tool for 3D TSV designs. MMI design services provide a plug-and-play solution. You need us if you absolutely, positively must make timing!

Micrologic Design Automation, Inc.
San Jose, CA
www.micrologic-da.com Booth: 910

Micrologic's nanoToolBox Accelerates Signoff with its interactive set of tools for backend DRC, RV and LVS verification. Our nanoToolBox is integrated with Cadence's Virtuoso and SpringSoft's Laker layout editors. Micrologic Design Automation, Inc. develops physical verification systems to detect and eliminate design violations early during IC layout design stages, enabling integrated circuit corporations to shorten time-to-market objectives, improving designs quality, reliability and performance.

COME AND VISIT US AT BOOTH 845

DATE 11

Grenoble, France
March 14 - 18, 2011

The 14th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day events consists of a conference with industry keynotes, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a management track. The scientific conference is complemented by a commercial exhibition showing state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms , embedded software, and industrial design experiences from different applications domains, such as automotive, aeropsace, wireless, telecom and multimedia applications. The organisation of user group meetings, fringe meetings, a university booth, research project demonstrations, a PhD forum, and social events offers a wide variety of opportunities to meet and exchange information on relevant issues for the design and test community.

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Please visit the DATE website for a list of the topics of interest for DATE 2011.

Submission of Papers

Papers can be submitted for standard oral presentation or for interactive presentation. All papers have to be submitted electronically by **September 5th, 2010,** via the conference web page: **www.date-conference.com**

Chairs

General Chair:
Bashir Al-Hashimi, University of Southampton, UK
Email: bmah@ecs.soton.ac.uk

Programme Chair:
Enrico Macii, Politecnico di Torino, IT
Email: enrico.macii@polito.it

DATE Secretariat - European Conferences, 3 Coates Place, Edinburgh EH3 7AA, United Kingdom
Tel: +44 131 225 2892 • **Fax:** +44 131 225 2925 • **Email:** sue.menzies@ec.u-net.com

EXHIBITING COMPANIES

Mirabilis Design Inc.
Sunnyvale, CA
www.mirabilisdesign.com Booth: 1250
Mirabilis Design provides easy to use graphical system simulation software and design methodology for the successful development of highly optimized electronics and embedded systems. The ultra-fast environment enables rapid exploration of key cost, power and performance design parameters allowing early converge to an optimal specification as it is being written and long before the development of RTL or embedded software. Time-to-first-results are accelerated using 100's of application templates and 400+ modeling components. The components library includes statistical resources, traffic generators, RegEx programming language and cycle-accurate hardware and software models.

Mixel, Inc.
San Jose, CA
www.mixel.com Booth: 416
Mixel is a leading provider of silicon-proven mixed-signal IP cores to the semiconductor and electronics industries. Mixel licenses high-performance analog and mixed-signal IP cores to the communications, consumer and storage markets for use in system-on-chip, ASICs and embedded systems. Mixel's mixed-signal IP portfolio includes high performance PHYs, SerDes, PLLs, DLLs, and analog building blocks, which are used in Mobile applications such as MIPI®, and MDDI, networking and storage applications such as PCI-Express, SATA, XAUI, Back-Plane, and Fibre-Channel.

MOSIS
Marina del Rey, CA
www.mosis.com Booth: 844
MOSIS enables IC designers with a faster, less risky route to commercialization by providing a single, expert access channel to world-leading foundries (IBM, TSMC, ON, AMS) and their advanced technologies (RF CMOS, SiGe BiCMOS, HV CMOS, etc). MOSIS services include - access to design kits and IP, technical support, MPW and LVP fabrication and packaging.

MunEDA GmbH
Munich, Germany
www.muneda.com Booth: 668
MunEDA provides leading EDA software technology for analysis, modelling and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA´s products and solutions enable customers to reduce the design times of their circuits and to maximize robustness, reliability and yield. MunEDA´s solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

Nangate
Sunnyvale, CA
www.nangate.com Booth: 1362
Nangate is an innovative developer of Electronic Design Automation (EDA) software and physical silicon intellectual property (IP) for Integrated Circuit design. Nangate offers software, IP and services for physical library IP creation, characterization, optimization and validation. Nangate provides a unique alternative to one-size-fits-all standard cell libraries and a low-risk alternative to custom library development or full-custom chip design to improve performance, power and area. Nangate's solution platform and IP integrates seamlessly with SoC design flows from the major EDA vendors.

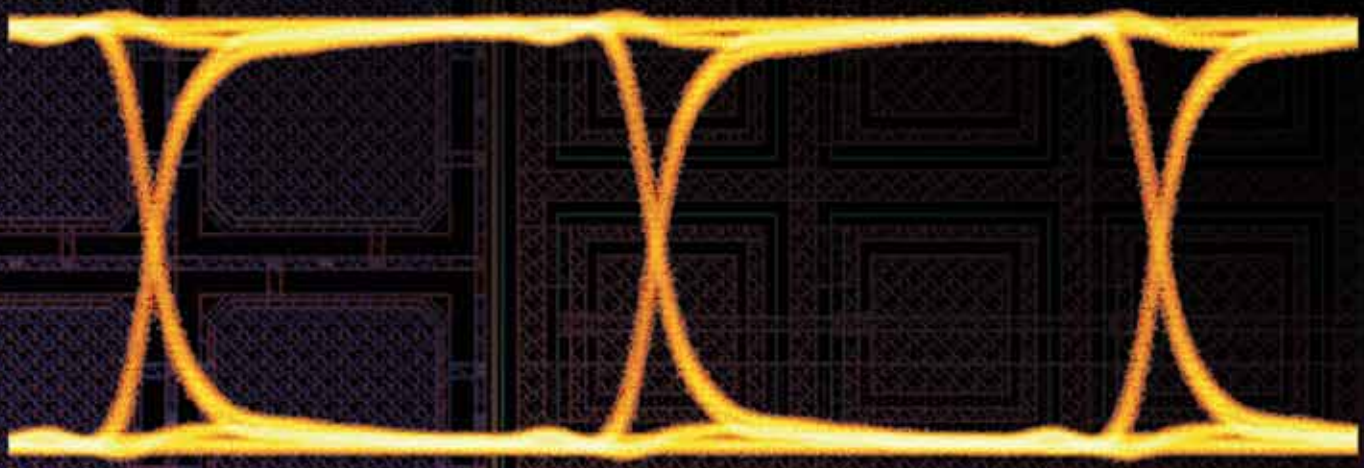
NEC Corp.
Kawasaki, Kanagawa, Japan
www.necst.co.jp/products/cwb/english/ Booth: 1641
CyberWorkBench (CWB) by NEC is a chip design platform based on an All-in-C" concept offering complete system LSI design tools all done in C. CWB is a complete design platform composed of a suite of tools such as behavioral synthesis, formal verification including equivalence prover and C-vs-RTL equivalence proverr, and simulation model creator. Its behavioral synthesis engine supports both control intensive and data dominant circuits. CWB is suitable for a wide range of applications: image processing, networking, filters, and control-logic modules."

NextOp Software, Inc.
Santa Clara, CA
www.nextopsoftware.com Booth: 1442
NextOp Software, Inc. is focused on delivering assertion-based verification solutions that allow design and verification teams to uncover bugs, expose functional coverage holes, and increase verification observability. NextOp's BugScope full-chip assertion synthesis solution is the first product to automatically generate whitebox assertions and functional coverage properties in SVA, PSL and Verilog to drive progressive, targeted verification via robust and executable design specifications; these properties are used to drive more effective verification in existing simulation, formal and emulation flows.

Oasys Design Systems, Inc.
Santa Clara, CA
www.oasys-ds.com Booth: 202
Oasys Design Systems RealTime Designer from Oasys re-imagines and re-creates logic synthesis with a solution so different that it has its own product category: Chip Synthesis. RealTime Designer is the first software for physical RTL synthesis of 100-million+ gate designs, able to synthesize RTL code to placed gates in a single pass much faster than traditional synthesis. It features a unique RTL placement approach that eliminates unending design closure and iterations between synthesis and layout. Interested? Stop by the Oasys booth for a demo.

OneSpin Solutions GmbH
Munich, Germany
www.onespin-solutions.com Booth: 1311
OneSpin's 360 MV® product family is the most comprehensive formal assertion-based verification (ABV) solution for RTL designs. It is the industry's only verification solution that provides an automatic, exhaustive coverage analysis, enabling users to efficiently find the intricate design and specification errors missed by other verification approaches confirmed in more than 300 projects. Visit Booth #1311 to see our tutorials covering X-verification, verification of complex arithmetic, verification of intricate control aspects using Operational ABV, and advanced processor verification.

Let Our Eyes Catch Yours™



Mobile
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- MIPI/MDDI Unified Solution
- MDDI

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- Frequency Synthesis
- Fractional-N
- Spread-spectrum
- De-skewing
- CDR

Storage & Networking
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- DisplayPort
- XAUI
- Fibre-Channel
- SATA
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- CE-ATA
- CardBus
- PATA
- DDR2
- SSTL
- HSTL
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Come visit us at DAC Booth # 416

EXHIBITING COMPANIES

OptEM Engineering Inc.
Calgary, AB, Canada
www.optem.com Booth: 1343
OptEM Engineering's software and services focus on interconnect design, extraction, modeling and analysis for high-speed analog, digital, and mixed-signal ICs and cable/connector systems. For deep-submicron ICs, the OptEM Inspector software provides layout-to-circuit device extraction, and 2D/3D substrate and interconnect RC extraction for detailed analysis of crosstalk and delay effects at the cell level. For cable/connector systems, the OptEM Cable Designer software models high-performance multi-conductor flex, twisted-pair, and specialty cables in telecommunication and data transmission applications.

Orora Design Technologies, Inc.
Redmond, WA
www.orora.com Booth: 813
Why search for FastSPICE with 10x speed up, while you can cut your mixed-signal simulation time by 100x to 1000x using the same simulator on the same test benches? Check out Orora's Arana, the industry-unique tool that automatically generates high-level behavioral models from a netlist. For a complete solution of automating analog design and verification, stop by to see Orora's Arche Custom-IC Verification and Characterization Platform and Arsyn Automated Circuit Design and Reuse Platform.

OVM World
www.ovmworld.org Booth: 1350
The Open Verification Methodology (OVM) is the industry's open and interoperable solution, guaranteed to run on multiple simulators, supporting multiple languages, and the basis for the Accellera UVM standard. The OVM enables scalability and reuse, fostering a vibrant verification ecosystem. OVMworld.org is the one-stop site for the OVM open-source library, documentation, and community contributions. Please join us in the OVM World booth for user and partner presentations, a live discussion by prominent verification experts, and a Tuesday cocktail reception.

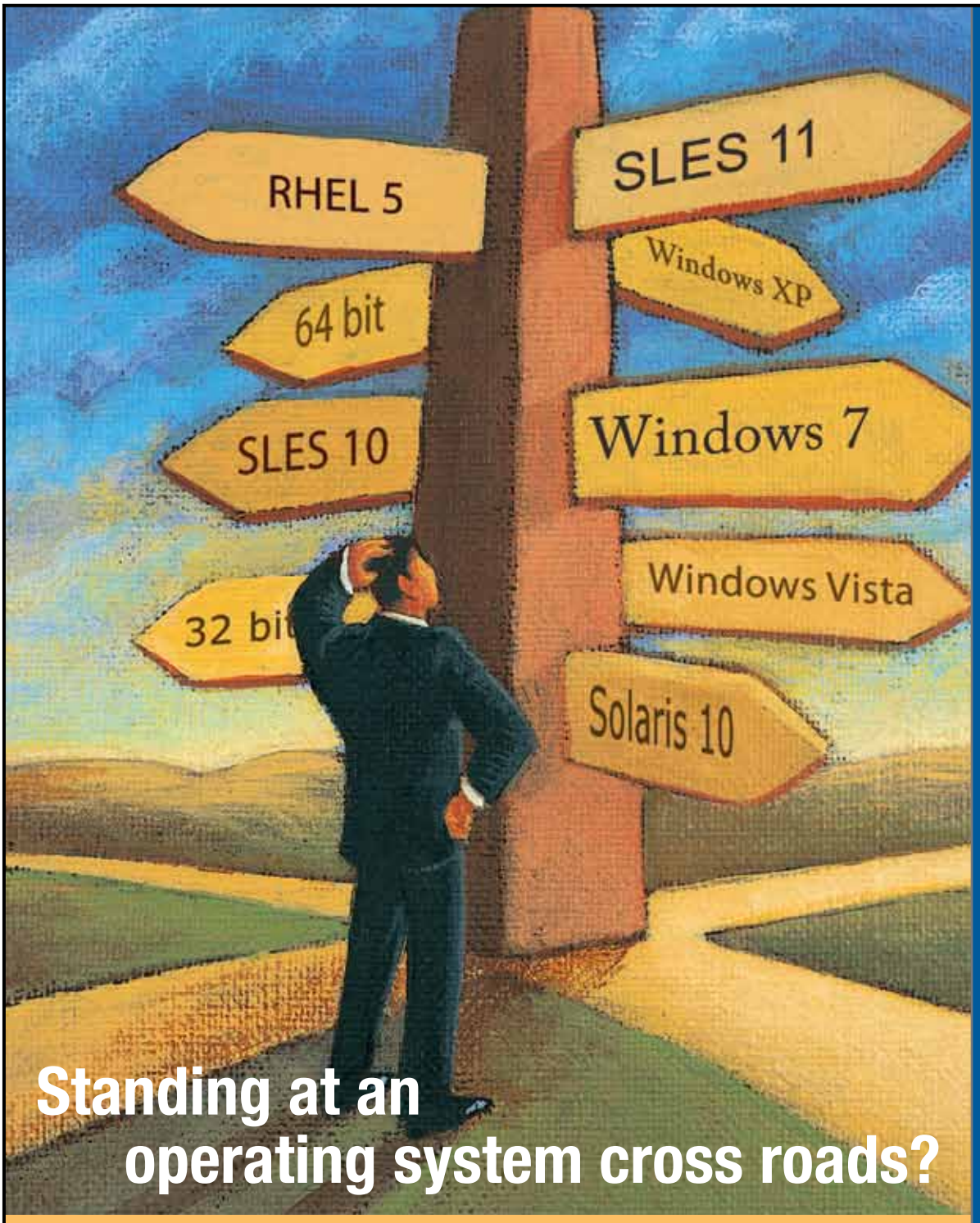
Physware, Inc.
Bellevue, WA
www.physware.com Booth: 180
Physware is a provider of high-speed 3D fullwave solutions that enable broadband verification and design across the chip-package-board ecosystems at unprecedented speed and capacity. Today, Physware helps customers solve their SI, PI, EMI and SNI challenges in a variety of design areas including memory, wireless RF systems, high-speed serial and parallel channels, FPGAs, analog systems and microprocessors. Speedups of 10x for SI and PI, and 100x for EMI over competing 3D field solutions are observed by several customers.

POLYTEDA Software Corp.
Mississauga, ON, Canada
www.polyteda.com Booth: 1301
POLYTEDA Software Corporation's PowerDRC/LVS offers fast and predictable performance for your largest designs today. Unlike other DRC tools, performance is not "design dependent". For any given node, performance is predictable based on the number of processors used in the verification process. One of many customer successes is a 4.4X verification speed up over the most common DRC product with matching QoR—for a baseband processor design. PowerDRC/LVS is a must see product at this year's DAC show.

Progate Group Corp.
Taipei, Taiwan
www.pgc.com.tw Booth: 1508
Founded in 1991, Progate Group Corporation (PGC), is a world-class leading ASIC design turnkey service provider. Being the first ASIC design turnkey service provider in Taiwan, we devote ourselves to provide the best quality of service to customers. In the past 19 years, PGC has successfully taped-out more than 950 projects and shipped millions of chips to worldwide customers since 1991. PGC provides gate array ASIC and structured ASIC which offer good solution for NRE cost-sensitive customers. In addition to the gate array and structured ASIC, PGC also provides excellent IP integration for SOC projects. From PCD-Express, SATA, DDRI & II to microprocessor and micro-controller, PGC provides customers with experience IP integration and Netlist-to-GDS II design turnkey service. PGC is dedicated to rapid delivery of cutting-edge ASIC solutions and shorten product time-to-design & time-to-market for customers worldwide. PGC is the certified member of Design Center Alliance (DCA) of TSMC.

Prolific, Inc.
Newark, CA
www.prolificinc.com Booth: 561
Prolific's products automate physical design optimization. ProPower® and ProTiming™ run after any place-and-route flow, reducing leakage power by 25%-70% on previously optimized designs, and improving TNS and WNS by an average of 10%. ProDFMOptimizer™ designs in manufacturability during the library creation process. ProGenesis® automatically produces standard cell layout, while our brand-new ProGenesis® Elite is designed for use at 22nm and below. Both reduce development time, allow architectural exploration, and automatically adapt to changes in design requirements or rules.

Pulsic Inc.
Santa Clara, CA
www.pulsic.com Booth: 468
Pulsic is the automation leader in custom digital and AMS design through production-proven floorplanning, placement, and routing software solutions for extreme design challenges at advanced nodes. Complementary to existing flows, standards, and databases, Pulsic technology delivers handcrafted quality, faster than manual design or general-purpose software solutions. Pulsic has delivered successful tapeouts at 40 nm and below for IDMs and fabless customers in the memory, FPGA, custom digital, LCD, imaging, and AMS markets worldwide.



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Need to know if your operating system will be supported by your Electronic Design Automation (EDA) supplier?

It's time to look at the map, the **EDA Industry OS Roadmap**! If you can use a guide through the complex operating system and platform pathways, the EDA Industry OS Roadmap is here to help you.

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EDA CONSORTIUM

EXHIBITING COMPANIES

R3 Logic Inc.
Waltham, MA
www.r3logic.com Booth: 1517
R3Logic, Inc., is the world leader in EDA tools for 3D system and IC design. In October 2007, in collaboration with Micro Magic, Inc., it announced the world's first commercial true-3D layout editor, MAX-3D. We will be demonstrating our latest version of the OpenAccess-based R3Integrator for 3D IP integration, featuring automated pin-to-TSV assignment, RDL routing, package and connectivity data importing, and physical vs. logical verification. R3Logic also provides design services to help you evaluate the benefits of 3D integration for your SoC's.

Rapid Bridge
San Diego, CA
www.rapidbridge.com Booth: 575
Rapid Bridge focuses on the application of its technology and services to solve the industry's dilemmas of cost, performance, power and time to market. The Technology Division focuses on the advancement and application of our patented technologies including LiquidIP™, LiquidASIC™, LiquidSoC™ and Core Power Reduction (CPR™) Technology. The Design Services Division delivers front-to-back digital design and chip design services for mixed-signal and SoC projects. Rapid Bridge's worldwide presence, exceptional combination of experience, expertise and technology access provides us with a unique ability to offer our clients a shorter time to market, unparalleled quality and overall value creation.

Real Intent, Inc.
Sunnyvale, CA
www.realintent.com Booth: 722
Real Intent, Inc. delivers verification confidence by providing automatic verification solutions for ASIC and FPGA designs. Through innovation and unique application of formal techniques, the Real Intent tools provide powerful solutions to important design and verification problems. Exhibited products at DAC include Ascent for early functional verification; Meridian for DFT and CDC verification; and PureTime for design constraints validation. In use at over 40 major customers worldwide, Real Intent tools help make the most complex designs possible.

Reed Business Information
Waltham, MA
www.reedbusiness.com Booth: 1302
EDN for more than 50 years has served the vital information needs of design engineers and engineering managers worldwide. The EDN franchise includes EDN, EDN Europe, EDN Asia, EDN China, and EDN Japan. EDN.com, the Internet home of EDN, delivers a three-dimensional view of the electronics industry via breaking news coverage, strategic business information, and in-depth technical engineering content.

RTC Group - EDA Tech Forum
San Clemente, CA
www.rtcgroup.com Booth: 1263
The RTC Group publishes three of the most read publications in the real-time and embedded computer arena - RTC Magazine, COTS Journal, and EDA Tech Forum. Our publications are focused on specific areas of the computer design industry, increasing our relevance and making our publications the most read in their prospective markets.

Runtime Design Automation
Santa Clara, CA
www.rtda.com Booth: 1349
RTDA offers an enterprise resource management tool suite: Workload Analyzer (simulation based compute farm planning), LicenseMonitor (license management and tracking), NetworkComputer (fast job scheduler), and FlowTracer (parallel design flow execution). These tools dramatically shorten design cycle times and improve the efficiency of design resources by taking revolutionary approaches to capacity planning and flow execution. CAD/IT managers can identify and eliminate bottlenecks or unused resources, or plan for new projects without having to run experiments on production systems, and can greatly shorten design cycles by running more tasks in parallel.

Sagantec
Santa Clara, CA
www.sagantec.com Booth: 542
Get on the fastest path to implementing your custom IP in a new process technology. Migrate analog and mixed-signal IP, library, memory, CPU and complete hierarchical designs to any foundry 65, 45 and 32 nm process technologies using Sagantec process migration automation tools. With an order of magnitude productivity combined with handcrafted quality and control, you can accelerate time to tape-out as well as improve reliability, EM and yield.

Sapient Systems
Fremont, CA
www.sapient-inc.com Booth: 375
Sapient's advanced software lets IC industry decision makers direct, optimize, plan and manage all aspects of product lifecycles, including market research, product planning, design, execution and discontinuance. Sapient's integrated framework encompasses data integration, predictive analytics and tradeoff analysis to estimate and evaluate target market size, requirements, schedules, and die economics (size, power, cost). This approach enables fast, accurate product planning and alignment to strategic, financial business objectives such as market share, profit margins, ROI and breakeven analysis.

Satin IP Technologies
Montpellier Cedex 2, France
www.satin-ip.com Booth: 610
Committed to design quality closure with fast return on investment, Satin IP Technologies delivers software solutions for fact-based design quality monitoring. Working within customers' design flows, VIP Lane® turns customers' design practices for IP blocks or SoCs into a robust set of quality criteria and automates the implementation and documentation of design quality metrics at no extra cost in engineering time or resources. VIP Lane shortens time-to-market by delivering effective flow integration and on-the-fly quality monitoring.

DESIGN AUTOMATION CONFERENCE

MANAGEMENT DAY

Where Business and Technology Intersect…

See page 10 for more details...

EXHIBITING COMPANIES

Seloco, Inc.
Seoul, Korea, Republic of
www.seloco.net Booth: 450
Since 1990, MyCAD offers a Windows-based EDA toolset installed in thousands of copies around the world – America, Europe, Asia recently including China and India. The main product for industrial application is MyChip Station, a set of IC layout editing and verification tools. MyCAD tools' economical, handy and practical features have encouraged small to medium size designs of ICs, LEDs, Opto-devices, MEMs, and LCDs recently. MyChip Station is also used to convert AutoCAD data to photolithographic mask data generation. A new feature is its added cross section view capability for an IC/device layout. MyCAD's educational tool set includes VHDL simulator/synthesizer, schematic capture/logic simulator, SPICE simulator and an FPGA experimental kit. Try free at www.mycad.com.

Semifore, Inc.
Mountain View, CA
www.semifore.com Booth: 1243
Semifore, Inc. provides the CSRCompiler, a tool that bridges the gap between hardware, software, verification, and documentation. The designer can specify the register address space of a design in a reusable manner to generate: Verilog and VHDL RTL; Verilog, or C headers; Perl, IEEE IP-XACT and Spirit SystemRDL; System Verilog for VMM and OVM; HTML web pages; and Adobe FrameMaker or Microsoft Office documentation. The specification is effortlessly available to the entire team to reduce cost and time to market.

Si2
Austin, TX
www.si2.org Booth: 502
Si2 is the largest organization of industry-leading semiconductor, systems, EDA and manufacturing companies focused on the development and adoption of standards to improve the way integrated circuits are designed and manufactured, in order to speed time-to market, reduce costs, and meet the challenges of sub-micron design. In our booth this year, member companies including AnaGlobe, Cadence, Pulsic, and Synopsys will be demonstrating products which implement the standards which Si2 member companies have developed.

Sigrity, Inc.
Campbell, CA
www.sigrity.com Booth: 1112
Sigrity provides advanced software analysis solutions to ensure power integrity and signal integrity in chips, packages and printed circuit boards; and physical design tools for single die and SiP implementations. Over 200 companies utilize Sigrity products as part of industry standard design flows. Sigrity solutions help companies overcome design challenges and get to market faster while avoiding costly respins and field failures. Sigrity products have won technology innovation awards and the company receives high marks for customer support.

Silicon Design Solutions
Milpitas, CA
www.silicondesignsolutions.com Booth: 573
SDS is an IP and Design Services Provider. Headquartered in Milpitas California USA Offering a wide range of Embedded Memories delivered as a Compiler or as a single Instance. SRAM, ROM, MPRF, CAM & TLB products available on Leading Foundry processes from 250nm to 28nm. Design Services include Custom Embedded Memory Compilers or Instances Optimized to meet Customer application, Complete Test Chip development, Bit Cell development and contracted augmentation of internal memory design teams. Engagement/Business Models are flexible and varied.

Silicon Frontline Technology
Campbell, CA
www.siliconfrontline.com Booth: 266
Silicon Frontline, the Silicon Proven extraction company, provides "Guaranteed Accurate" post-layout verification software for improving design quality and reliability. With over 200 designs verified, features include high performance, full-chip parasitic extraction, integration with standard flows and foundry endorsements. We will discuss F3D (Fast 3D extraction) enhancements for extraction of high precision analog and new R3D (Resistive 3D extraction) analysis capability for optimizing power device designs.

SKILLCAD Inc.
San Jose, CA
www.skillcad.com Booth: 782
SKILLCAD is dedicated to custom routing and productivity enhancement tools for IC layout design. SKILLCAD is seamlessly integrated with Cadence Virtuoso Layout Platform, supporting both IC5.x and IC6.x. SKILLCAD introduces convenient ways for bus/path routing, shield wiring, auto via filling, pin labeling dummy pattern filling, slot hole cutting and many other handy features. SKILLCAD uniVia compiler handles 32nm below via design rules such as rectange vias, various via patterns and multiple DFM design rules. SKILLCAD has a growing list of customers in RF/FPGA/CMOS Sensor/Power IC/Memory/Analog Mixed Signal designs.

Solido Design Automation Inc.
San Jose, CA
www.solidodesign.com Booth: 381
Solido Design Automation enables Variation-Aware Custom IC Design for analog/RF, IO, memory and standard cell digital library designers. Solido Variation Designer is a fast, sign-off accurate, high capacity tool suite that improves design performance, parametric yield, and designer productivity by analyzing variation impact on design specifications, identifying transistor sensitivities to variation effects, and fixing the design to meet specifications. Solido uses foundry models to address variation caused by process and environmental (PVT) corners, global and local random variation, and proximity effects.

WELCOME TO THE WORLD OF USER TRACK!

TUESDAY, JUNE 15 - THURSDAY, JUNE 17

The DAC User Track brings together IC designers from across the globe. The technical program offers a unique opportunity to pick up the latest tips and tricks from the industry expert IC designers. UT features over 110 presentations on a wide variety of EDA topics. There is no other way to improve your 'design IQ' in just a short amount of time.

SEE PAGES 31-37 FOR DETAILS

DESIGN AUTOMATION CONFERENCE

EXHIBITING COMPANIES

Sonnet Software, Inc.
N. Syracuse, NY
www.sonnetsoftware.com Booth: 150
Sonnet Software provides high frequency electromagnetic (EM) software for 3D planar circuit and component model extraction. The Sonnet Suites are aimed at today's demanding design challenges involving predominantly planar circuits and antennas (including microstrip, stripline, coplanar waveguide, PCB (single and multiple layers) and RF packages incorporating any number of layers of metal traces embedded in stratified dielectric material. Sonnet integrates with most major EDA design flows. Visit Booth 150 for information on Sonnet's software and get a sneak preview of our upcoming Release13.

Springer
New York, NY
www.springer.com Booth: 549
Find Springer—with nearly 200 NEW books on hand and nearly 500 more on virtual display—at booth 549.

SpringSoft, Inc.
San Jose, CA Silver Exhibitors
www.springsoft.com Booth: 1357
SpringSoft specializes in unique automation technologies for design and verification. Its Verification Enhancement solutions are comprised of the Verdi™ Automated Debug System that cuts debug time in half and the new Certitude™ Functional Qualification System that helps you get closer to verification closure. Its Custom IC Design solutions deliver unsurpassed controllable layout automation with the Laker™ Custom Layout Automation System and new Laker Custom Digital Router and Laker Custom Row Placer. Visit us at booth #1357 to learn more.

StarNet Communications
Sunnyvale, CA
www.starnet.com Booth: 944
StarNet is taking remote EDA tool access to a new level of mobility with iLIVE the latest in a suite of remote host access solutions. iLIVE runs on Apple iPads and lets engineers work productively and securely while away from their office.

Synapse Design
San Jose, CA
www.synapse-da.com Booth: 528
Synapse Design is the preferred Design Partner for an extensive array of large fortune 500 companies, worldwide. Our engagement model is flexible all the way from full-scale managed projects to placing individuals or teams on site on a contracted, hourly basis. We support our clients across a broad spectrum of skill sets in both hardware and software design, from device level to full system development.

Synchronicity - see Dassault Systèmes
Lowell, MA
www.3ds.com Booth: 1370
See Dassault Systemes

Synfora, Inc.
Mountain View, CA
www.synfora.com Booth: 770
Synfora is the premier provider of high level synthesis tools used to design complex SoCs and FPGAs. The PICO C/C++ synthesis platform offers designers 2x to 5x productivity gains by creating application accelerators from an untimed C algorithm. PICO products provide the best productivity using the highest level of abstraction; yield QoR competitive with manual design and enable high-level verification giving access to 100x simulation speed-ups. Synfora serves customers worldwide in the audio, video, imaging, wireless, and security segments.

Synopsys, Inc. – Common Platform Access Innovation
Mountain View, CA Platinum Exhibitors
www.synopsys.com Booth: 586
Synopsys – Common Platform Access Innovation Booth
- ARM - www.arm.com
- Common Platform - http://www.commonplatform.com/
- GLOBALFOUNDRIES – http://www.globalfoundries.com/
- IBM - http://www-03.ibm.com/technology/
- Samsung - http://www.samsung.com/us/business/components/semiconductor
- Synopsys - www.synopsys.com

This booth is dedicated to the unique design enablement collaboration between ARM, Common Platform (GLOBALFOUNDRIES, IBM, Samsung Electronics) and Synopsys. Leveraging our industry leadership, this collaboration is enabling proven design enablement solutions for optimizing innovation and accelerating your design with best-in-class technology, physical and processor IP and tool/flow solutions for the Common Platform's 32nm/28nm high-k metal-gate (HKMG) process technology.

Synopsys, Inc. - System-level Solutions
Mountain View, CA
www.synopsys.com Booth: 581
Visit the Synopsys System-level Solutions booth #581 during the Design Automation Conference where you can learn more about our comprehensive suite of tools for accelerating and improving embedded system development and verification. The unique combination of architecture exploration, FPGA synthesis, DSP algorithm design and high-level synthesis, IP, and virtual and hardware prototyping platforms provide developers with the most complete system-level and prototyping solutions for today's software-intensive, multicore designs resulting in significantly reducing your time to market.

Synopsys, Inc. - Corporate
Mountain View, CA
www.synopsys.com Booths: 595, 597
Synopsys, Inc. is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of system-level, implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification, virtual prototyping for embedded software development and time-to-results.


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Attend the DAC Workshop for Women in Electronic Design to hear Patty Azzarello explain why some get ahead, why some don't, and what you can do about it.
WWED
Monday, June 14, 2010
11:30 AM – 2:00 PM
Room 204C
DAC Workshop: More Than Core Competence... What it Takes for Your Career to Survive, and Thrive! Hosted by Women in Electronic Design
See page 43 for details...
DESIGN AUTOMATION CONFERENCE
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EXHIBITING COMPANIES

Synopsys, Inc. - Standards Booth
Mountain View, CA
www.synopsys.com Booth: 585
The Standards Booth
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Teamwork + Standards + Interoperability = Your Success
Interoperability based on open standards and teamwork leads to greater productivity for successful design projects. Synopsys, a world leader in software and IP for semiconductor design, verification and manufacturing, dedicates this booth to industry standards that provide increased productivity, reduced cost and improved EDA interoperability that engineers demand. See the latest advancements in Power Architecture technology, systems, open verification, and analog/custom standards and ecosystems in the industry.

SynTest Technologies, Inc.
Sunnyvale, CA
www.syntest.com Booth: 522
Since 1990, SynTest has developed and commercialized many market-leading design-for-test (DFT) products, including Logic/Memory BIST (TurboBIST), Scan/ATPG (TurboScan), test compression (VirtualScan), and fault simulation (TurboFault). SynTest's DFT IP, e.g., at-speed scan/BIST, are silicon-proven and protected by a rich portfolio of 40+ patents. The TurboBIST-Logic product is used today by leading companies to reduce test-cost and improve quality. The newly released MULTICORE feature dramatically improves ATPG performance using multicpu systems. SynTest tools are backed by the most dedicated support team.

Tanner EDA
Monrovia, CA
www.tannereda.com Booth: 1342
Tanner EDA provides Windows and Linux based EDA software solutions that drive innovation for the design, layout and verification of analog and mixed-signal ICs and MEMS. Tanner EDA's HiPer Silicon is a complete IC design suite that encompasses schematic capture, circuit simulation, waveform probing, physical layout, foundry-compatible DRC, extraction, and verification. Tanner EDA products enable faster time to market, lower costs, and shorter design cycles and are used to develop devices in the biomedical, consumer electronics, next-generation wireless, imaging, power management and RF markets.

Target Compiler Technologies NV
Leuven, Belgium
www.retarget.com Booth: 1376
Target is the leading provider of software tools used to accelerate and optimize the design and programming of application-specific processor cores (ASIPs). ASIPs are used to build multicore SoCs for demanding embedded applications - including co-processors, accelerators and programmable datapaths. Target's "IP Designer" tool-suite enables designers to create ASIPs with the right balance between performance, low power/cost, and flexibility. IP Designer has been applied by customers worldwide for diverse application domains, including GSM/WCDMA/HSDPA handsets, VoIP, audio/video/image codec/processing, automotive, ADSL/VDSL modems, wireless LAN, hearing instruments, and mobile/low-power applications.

Teklatech
Copenhagen, Denmark
www.teklatech.com Booth: 341
Teklatech is innovating solutions for dynamic power optimization. Our technologies enable the semiconductor industry to increase design efficiency and achieve faster backend convergence with less iterations and faster time-to-market. Teklatech's FloorDirector reduces on-chip dynamic peak current significantly, working on a post-synthesis netlist level. FloorDirector is a key design methodology improvement for any semiconductor company doing digital and mixed-signal design seeking to systematically reduce dynamic IR Drop, EMI and digital substrate noise.

Tela Innovations
Los Gatos, CA
www.tela-inc.com Booth: 380
Tela Innovations offers innovative, lithography optimized design solutions that lower power, reduce die area and improve performance of integrated circuits in advanced technologies. With the acquisition of Blaze, Tela adds additional capability to its line up aimed specifically at reducing leakage power. This technology will compliment Tela's solution of on-grid, straight line, one dimensional layout structures. These lithography-optimized structures enable manufacturing process optimization resulting in significant improvements in performance, power and area.

Tiempo
Montbonnot St Martin, France
www.tiempo-ic.com Booth: 710
Tiempo delivers an innovative approach to low power design with IP cores and design tools that leverage its patented clockless, delay insensitive technology. Its solutions, which include microcontroller and cryptoprocessor cores, can be implemented using standard EDA tools and input formats, and address critical performance, security and PVT variation requirements in a wide range of applications. Tiempo will present live demos of ACC (Asynchronous Circuit Compiler) and TAM16 (Tiempo 16-bit microcontroller).

TOOL Corp.
Tokyo, Japan
www.tool-corp.com Booth: 189
TOOL Corp. offers EDA tools and innovative solutions to meet your IC design needs. Showcased is LAVIS, a layout viewer not only allows displaying of VLSI data quickly but also provides rich functionality for visual validation in timing closure, layout verification, lithography verification, and failure analysis. Also introduced is OASIS-Utility, a unique set of modules including a fast hierarchical data checker against rigorous custom sign-off regulations. Using LAVIS and OASIS-Utility can minimize risks in data logistics situations through quick verification of illegal data.

True Circuits, Inc.
Los Altos, CA
www.truecircuits.com Booth: 1356
True Circuits, Inc. (TCI) is the leading provider of timing IP for the semiconductor, systems and electronics industries. TCI develops robust state-of-the-art circuits using a methodical and proven design strategy and in close association with the world's leading fabs, IDMs and design service providers. TCI offers a complete family of high quality, low-jitter and standardized PLLs and DLLs in a range of frequencies, multiplication factors, sizes and functions in TSMC, UMC, CHRT and Common Platform processes from 180nm to 40nm.

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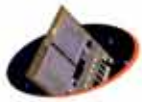

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EXHIBITING COMPANIES

TSMC

San Jose, CA

Gold Exhibitors

www.tsmc.com/dac/default.htm

Booth: 294

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry's largest portfolio of process-proven libraries, IPs, design tools and reference flows. The Company's managed capacity in 2009 totaled 9.96 million (8-inch equivalent) wafers, including capacity from two advanced 12-inch GIGAFABs™, four eight-inch fabs, one six-inch fab, as well as TSMC's wholly owned subsidiaries, WaferTech and TSMC China, and its joint venture fab, SSMC. TSMC is the first foundry to provide 40nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan.

TSMC Open Innovation Forum, Apache

San Jose, CA

www.apache-da.com

Booth: 294

Apache provides industry's leading power and noise solutions for chip-package-system convergence from RTL to sign-off. Apache's products address the critical power noise challenges associated with specific design domains such as digital, analog/mixed-signal, package/PCB, and SiP/3D-IC, while providing an eco-platform that integrates the SoC, Custom IP, and System worlds. From RTL power analysis and reduction, to early stage prototyping and optimization, and through chip and package sign-off, Apache's products enable designers to reduce power, increase performance, lower cost and mitigate risk.

TSMC Open Innovation Forum, Cadence

San Jose, CA

www.cadence.com

Booth: 294

Cadence and TSMC have collaborated for over 2 decades to maximize quality of results for power, performance and manufacturability to meet time-to-volume requirements. TSMC Reference Flow 11 will show unique capabilities such as C-to-Silicon, 3D-IC design and DFM with golden embedded engine for advanced nanometer SoC implementation from system-to-silicon successfully. Integrated Signoff Flow for 65nm, RF Reference Kit and Analog Mixed-Signal Reference Flow recently released by TSMC and Cadence deliver predictable, high quality and production-proven flows for mixed-signal SOC designs.

TSMC Open Innovation Forum, eSilicon

Sunnyvale, CA

www.esilicon.com

Booth: 294

eSilicon, a pioneering semiconductor Value Chain Producer (VCP), provides a comprehensive suite of design, productization and manufacturing services, enabling a flexible, low-cost, lower-risk path to volume chip production. The company delivers application specific integrated circuits (ASICs) to system original equipment manufacturers (OEMs) and fabless semiconductor companies who serve a wide variety of markets including the consumer, computer, communications and industrial segments.

TSMC Open Innovation Forum, Helic, Inc.

San Francisco, CA

www.helic.com

Booth: 294

Helic, Inc. develops disruptive EDA technology for RFIC and System-in-Package design. We provide our customers with a service model combining EDA tools, IP and services, enabling first-pass silicon while greatly reducing the development cycles of integrated wireless transceiver products. VeloceRF™ is our leading EDA tool for integrated inductor synthesis, modeling, and verification. Helic's products have been adopted by many renowned semiconductor companies worldwide, with over 500 designers using our tools.

TSMC Open Innovation Forum, Integrand

Berkeley Heights, NJ

www.integrandsoftware.com

Booth: 294

Integrand Software, Inc. provides tools to design high frequency, RF/Mixed Signal ICs for the semiconductor and electronics industries. Our advanced full-wave 3D EM simulation tool, EMX, is fast, accurate and easy to use. It is 10-50 times faster and handles problems several times larger than other commercial EM tools. The world's top four foundries use EMX to develop scalable models for their design kits. Many major IC companies use EMX for designing inductors, transformers, MiM/MoM capacitors, VCOs, LNAs and filters.

TSMC Open Innovation Forum, Lorentz

Santa Clara, CA

www.lorentzsolution.com

Booth: 294

Lorentz Solution, Inc., based in Santa Clara, California, is a growing EDA company providing an unique electromagnetic (EM) simulation-based design and verification environment to enable analog RF IC designers to design, analyze and eliminate high frequency effects early in their circuit design process. Its flagship product, PeakView, is adopted by RF/wireless, analog, foundry and FPGA companies in the world. These companies chose PeakView because of its unique Layout EM (LEM), highly efficient PCircuit and flexible simulation model generation, tightly integrated in Cadence environment. PeakView is proven and ready for tomorrow advanced processes in all major foundries.

TSMC Open Innovation Forum, Magma

San Jose, CA

www.magma-da.com

Booth: 294

Since 1997, Magma has been shaking up the EDA industry with groundbreaking software that saves time, effort and money while delivering better results. Visit us at the TSMC Open Innovation Forum to learn more about Magma's mixed-signal SoC solutions. Our Titan mixed-signal platform enables interoperability using TSMC's iPDK and AMS reference flow. Our Talus digital implementation platform is included in TSMC's Reference Flows and provides advanced techniques for 28-nm, low-power and DFM challenges. Check us out - we're rock'n your world – again.

A Powerful Platform for Amazing Performance

Performance. To get it right, you need a foundry with an **Open Innovation Platform™** and process technologies that provides the flexibility to expertly choreograph your success. To get it right, you need TSMC.

Whether your designs are built on mainstream or highly advanced processes, TSMC ensures your products achieve maximum value and performance.

Product Differentiation. Increased functionality and better system performance drive product value. So you need a foundry partner who keeps your products at their innovative best. TSMC's robust platform provides the options you need to increase functionality, maximize system performance and ultimately differentiate your products.

Faster Time-to-Market. Early market entry means more product revenue. TSMC's DFM-driven design initiatives, libraries and IP programs, together with leading EDA suppliers and manufacturing data-driven PDKs, shorten your yield ramp. That gets you to market in a fraction of the time it takes your competition.

Investment Optimization. Every design is an investment. Function integration and die size reduction help drive your margins. It's simple, but not easy. We continuously improve our process technologies so you get your designs produced right the first time. Because that's what it takes to choreograph a technical and business success.

Find out how TSMC can drive your most important innovations with a powerful platform to create amazing performance. Visit **www.tsmc.com**

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EXHIBITING COMPANIES

TSMC Open Innovation Forum, Mentor
Wilsonville, OR
www.mentor.com Booth: 294
Mentor Graphics is a world leader in EDA products and consulting services for semiconductor companies. Mentor offers solutions that meet the demand for short design cycle time, improved engineering productivity, and optimized yield. The Mentor implementation flow is fully qualified under TSMC's Reference Flow 10 for 28nm and larger processes and includes the Olympus-SoC place and route system, the Calibre physical verification suite, Calibre DFM solutions to address random and systematic issues affecting yield, and the comprehensive Tessent suite for production and built-in self test, failure diagnosis and accelerated yield learning.

TSMC Open Innovation Forum, MoSys
Sunnyvale, CA
www.mosys.com Booth: 294
MoSys, Inc. develops serial chip-to-chip communications solutions that deliver unparalleled bandwidth performance for next generation networking systems and advanced SoC designs. MoSys' IP portfolio includes DDR3 PHYs and SerDes IP supporting data rates from 1 - 11 Gbps across a variety of standards in addition to its flagship 1T-SRAM® technology. MoSys IP offers a combination of high-density, low power consumption, high speed and low cost advantages and is production-proven in more than 225 million devices.

TSMC Open Innovation Forum, Silicon Frontline
Campbell, CA
www.siliconfrontline.com Booth: 294
Silicon Frontline, the Silicon Proven extraction company, provides "Guaranteed Accurate" post-layout verification software for improving design quality and reliability. With over 200 designs verified, features include high performance, full-chip parasitic extraction, integration with standard flows and foundry endorsements. We will discuss F3D (Fast 3D extraction) enhancements for extraction of high precision analog and new R3D (Resistive 3D extraction) analysis capability for optimizing power device designs.

TSMC Open Innovation Forum, Solido
San Jose, CA
www.solidodesign.com Booth: 294
Solido Design Automation enables Variation-Aware Custom IC Design for analog/RF, IO, memory and standard cell digital library designers. Solido Variation Designer is a fast, sign-off accurate, high capacity tool suite that improves design performance, parametric yield, and designer productivity by analyzing variation impact on design specifications, identifying transistor sensitivities to variation effects, and fixing the design to meet specifications. Solido uses foundry models to address variation caused by process and environmental (PVT) corners, global and local random variation, and proximity effects.

TSMC Open Innovation Forum, SpringSoft
San Jose, CA
www.springsoft.com Booth: 294
SpringSoft specializes in unique automation technologies for design and verification. Its Laker™ Custom IC Design solutions offer the power of controllable automation and unmatched interoperability to achieve superior layout results with less effort for analog, mixed-signal, and custom digital designs. Visit us to see our latest solutions, Laker Custom Digital Router and Laker Custom Row Placer.

TSMC Open Innovation Forum, Synopsys
Mountain View, CA
www.synopsys.com Booth: 294
Synopsys is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk.

TSMC Open Innovation Forum, Tela Innovations
Campbell, CA
www.tela-inc.com Booth: 294
Tela Innovations offers innovative, lithography optimized design solutions that lower power, reduce die area and improve performance of integrated circuits in advanced technologies. With the acquisition of Blaze, Tela adds additional capability to its line up aimed specifically at reducing leakage power. This technology will compliment Tela's solution of on-grid, straight line, one dimensional layout structures. These lithography-optimized structures enable manufacturing process optimization resulting in significant improvements in performance, power and area.

TSMC Open Innovation Forum, Virage Logic
Fremont, CA
www.viragelogic.com Booth: 294
Virage Logic is a leading provider of semiconductor IP for the design of complex integrated circuits. The company's highly differentiated product portfolio includes embedded SRAMs, embedded NVMs, embedded memory test and repair, logic libraries, memory development software, and interface IP solutions. As the industry's trusted semiconductor IP partner, foundries, IDMs and fabless customers rely on Virage Logic for higher performance, lower power, higher density, optimal yield, shortened time-to-market and time-to-volume.

TSSI - Test Systems Strategies, Inc.
Beaverton, OR
www.tessi.com Booth: 1505
Founded in 1979, TSSI is the world leader in design-to-test conversion and validation software solutions, and a leader in turnkey test engineering services. 1. Pattern Conversions: 30+ EDA formats to all leading ATE formats; 2. Pattern Validations: ATE patterns to Verilog testbench; ATE to other ATE formats; and VirtualTester solution to simulate ATE patterns as-is; 3. Test Engineering Training and Services: digital/mixed-signal and RF test program development; wafer sort; final test; silicon debug; yield enhancement; and test throughput optimization.

EXHIBITING COMPANIES

Tuscany Design Automation, Inc.
San Jose, CA
www.tuscanyda.com Booth: 1584

Don't let critical design metrics go unnoticed! Insufficient, inaccurate, and late information slips tapeouts. Tuscany's web-based dashboard gives you instant access to the most current design information, from across the hall or around the world. Managers can identify problem blocks with visual summaries of all of the data, and designers can review and share the detailed physical layout of a specific critical timing path… all in one place. All this, even with an iPad. Register to win one.

UMIC Research Centre
Aachen, Germany
www.umic.rwth-aachen.de Booth: 377

UMIC is a research cluster established under the German Federal and State Government Excellence Initiative. Its focus is on Ultra high-speed Mobile Information and Communication supporting the demands of future mobile applications and systems. Being an academic research centre with strong links to wireless industry and mobile network operators, activities cover research on basics concepts and new paradigms, on key solutions and tools, the development of prototypes and demonstrators, and the technology transfer to industry.

Uniquify, Inc.
Santa Clara, CA
www.uniquify.com Booth: 177

Uniquify Inc. provides leading edge complete ASIC design (Spec to GDSII) and IP solutions focusing on complex multi-million gate System-on-Chip designs. The company has a proven track record of successful tapeouts in joint SoC development projects leveraging 28/32nm, 40nm, 65nm, and 90nm technology nodes and Uniquify's Perseus Design Framework. ASIC Design Services:

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- Logic verification
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- Customizable DDRC 2133A – DDR2/DDR3 Memory Controller
- mDDRC 400A- Mobile Memory Controller
- PHY 2133A- DFI Compliant DDR PHY with SCL™ technology
- AXI 1066A- AXI Bus Interface
- AHB 1066A- AHB Bus Interface
- DDLL 1066A- Digital Delay Locked-Loop

Univa UD
Austin, TX
www.univaud.com Booth: 772

Univa UD is a leading provider of cloud management software. Companies worldwide use our award-winning products to build and manage internal cloud environments, leverage public cloud services, and enable cloud service offerings. We offer the widest available range of production-ready cloud management software, including infrastructure management and service governance. For over a decade, Univa products have delivered measurable business value to organizations of all kinds by reducing costs, increasing resource utilization, and optimizing the computing environment.

Vennsa Technologies, Inc.
Toronto, ON, Canada
www.vennsa.com Booth: 250

Debugging RTL failures is the major manual burden in the verification cycle today. Vennsa OnPoint™ is the industry's first and only automated debugging tool that localizes the source of errors with no user guidance. It automatically points engineers to the root cause of failure and also suggests how to fix the bugs. OnPoint's revolutionary technology picks-up where verification tools leave off. OnPoint has proven to improve productivity, saving weeks or months of effort and guaranteeing a faster design closure.

Verific Design Automation
Alameda, CA
www.verific.com Booth: 378

Verific Design Automation provides the (System)Verilog and VHDL front-ends for a majority of EDA and FPGA tools. When you are parsing RTL, the software is likely to come from Verific. Find out why Xilinx, Actel and Altera, Synopsys, SpringSoft and Magma, and 40+ others utilize Verific. It's giraffic!

Veritools, Inc.
Los Altos, CA
www.veritools.com Booth: 544

Veritool's powerful RTL Verilog/SystemVerilog/VHDL source code debugging and waveform display software, version ut2k10.1.2, is now enhanced with a new internal data base, the new ULTRA mode, that provides 3-12 times faster load and display speeds for both digital and analog waveform data, and includes a built in SystemVerilog Assertion simulator. New features include more than 3 X faster VCS speeds for designers with Verilog/SystemVerilog designs, and new data format readers so test engineers can directly read and display their WGL and STIL files and rerunning analog measures without re-simulation.

WinterLogic Inc.
Roseville, MN
www.winterlogic.com Booth: 421

WinterLogic specializes in development of a functional fault simulator and fault simulation environment for Verilog designs. Our Z01X fault simulator, based on our proprietary C2 algorithm, is the fastest and most memory efficient fault simulator available. Its integrated Expert Test System uses "testability analysis" to provide optimum test ordering, elimination of redundant tests and test specific fault selection, making fault simulation of large designs a reality.

X-FAB Semiconductor Foundries
Erfurt, Germany
www.xfab.com Booth: 1408

X-FAB is the leading analog/mixed-signal foundry group manufacturing silicon wafers for analog-digital integrated circuits. A specialty foundry for "More than Moore" technologies, X-FAB provides a clear alternative to typical foundry services by combining solid, specialized expertise in advanced analog and mixed-signal process technologies with excellent service and first-class technical support. Wafers are manufactured on advanced modular CMOS and BiCMOS processes from 1.0 to 0.18 µm, and special BCD, SOI and MEMS long-lifetime processes. X-FAB maintains four wafer production facilities in Germany, the US and Malaysia.

EXHIBITING COMPANIES

XJTAG
Cambridge, United Kingdom
www.xjtag.com Booth: 268
XJTAG is a producer of hardware and software boundary scan products. XJTAG's products help engineers accelerate the circuit design and development from early in the design stage right through to manufacture and servicing. So if you design boards with BGA's, have hardware that include FPGA's, CPLDs, DSPs or microprocessors and you would like to debug your boards, detect faults and prove your design quickly and easily then XJTAG can most probably help you. Visit Booth 267.

XYALIS
Grenoble, France
www.xyalis.com Booth: 162
XYALIS, the specialist of layout finishing, presents the most complete mask data preparation solution: an integrated suite of tools automating the most challenging steps of mask creation: advanced frame generation, Multi-Project Wafer assembly, optimized wafer map, and mask set generation supporting multi-layer reticles and 1X masks. A universal SEMI-P10 compliant mask management database warrants error free supplier-independent mask ordering. This mask data preparation solution reduces time to manufacturing, increases manufacturing yield, and eliminates errors during mask and wafer production.

Z Circuit Automation
Mountain View, CA
www.z-circuit.com Booths: 470, 462
Z Circuit specializes in EDA software for advanced circuit analysis and cell library development. Z Circuit will show ground-breaking new technology and major new testimonials. ZCHAR is a sophisticated all-in-one system for cell library characterization of standard cell, memory, IO pad, and custom cells. ZChar provides breakthrough performance and configurability to handle a wide range of cells. Z Circuit Library Analyzer may be a great addition for you, if you already have an existing cell library characterization system in place.

Zocalo Tech, Inc.
Austin, TX
www.zocalo-tech.com Booths: 1509, 1503
ZOCALO TECH ..... MAKING ASSERTION BASED VERIFICATION WORK FOR YOU! Zazz ™ from Zocalo Tech has been architected and developed from the ground up with one goal in mind – increased productivity for engineers adopting and utilizing Assertion Based Verification. Learn how Zazz enables this game changing verification technology by solving the issues that have kept ABV from wide spread acceptance. Booth Number 1509 and Suite No. 1503.
Contact hmartin@zocalo-tech.com to set up a private demo.

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Cary, NC
www.conventor.com Booth: 269

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www.elastix-corp.com Booth: 753
Discover the benefits unlocked by extracting your design's natural frequencies through elastic clocks. Run faster or lower power by as much as 35%, dramatically reduce timing margins, and adapt to PVT variability like never before. Experience unprecedented design robustness during voltage droops and emergencies. Achieve all of this with your existing tools and flows with miniscule area overhead. Elastix offers a head start in what promises to emerge as the next wave of deep sub-micron design practices.

Posedge
Sunnyvale, CA
www.posedge.com Booth: 1466
Posedge Inc. headquartered in Sunnyvale, CA, USA, is leading supplier of Wired / Wireless Secure Networking Semiconductor Intellectual Property ("IP") solutions for SOC/FPGA. Posedge's highly differentiated product portfolio includes Multi-Gigabit Layer2+ Switch, 10Gbps Data Compression Engine, 10 Gbps MACsec engine, TCP Offload Engine, IPSEC Protocol Processor, Multi-Gigabit Routing Processor in addition to SoC Solutions such as SD / SDIO, Flash and Bus Protocols. Posedge's solutions include hardware, software drivers, firmware, software stacks as applicable and the IP is augmented with leading-edge design and verification Services for customization.

TSMC Open Innovation Forum, Analog Bits
Mountain View, CA
www.analogbits.com Booth: 294
Analog Bits, Inc. specializes in designing transistor level IP components fully customized for easy and reliable integration into modern CMOS digital chips. Products include precision clocking macros such as PLLs, DLLs, programmable interconnect solutions such as multi-protocol SERDES, DDR/programmable I/Os and specialized memories such as high-speed SRAMs, T-CAMs. With billions of IP fabricated in customer silicon from 0.25-um to 28-nm processes, Analog Bits is the premier IP supplier at TSMC with an outstanding heritage of "first time working silicon" at numerous processes geometries including custom processes.

MERGERS, ACQUISITIONS AND NAME CHANGES

CoWare, Inc. ..... see Synopsys, Inc.
LogicVision, Inc. ..... see Mentor Graphics Corp.
QThink, Inc. ..... see Rapid Bridge, LLC
Sequence Design, Inc. ..... see Apache Design Solutions, Inc.
VaST Systems Technology Corp ..... see Synopsys, Inc.
Zeland Software, Inc ..... see Mentor Graphics Corp.

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48TH CALL FOR CONTRIBUTIONS

48TH DESIGN AUTOMATION CONFERENCE

San Diego Convention Center, San Diego, CA June 5-10, 2011

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With a heritage of excellence for almost half a century, DAC continues to be the premier conference devoted to Electronic Design Automation (EDA) and the application of EDA tools in designing advanced electronic systems. DAC 2011 is seeking papers that deal with tools, algorithms, and design techniques for all aspects of electronic circuit and system design. We invite submissions in the following categories:
Research papers, User Track papers, "Wild and Crazy Ideas" (WACI) topic papers, suggestions for special sessions, panels, and tutorials, and proposals for workshops and colocated events. Submissions must be made electronically at the DAC website. Detailed guidelines for all categories are available on the DAC website.
Focus Areas: Apart from the core Electronic Design Automation topics, DAC specifically solicits Research papers in the areas of design automation for many-core architectures, system prototyping technology and embedded software design and debug.

RESEARCH PAPERS

DUE BEFORE 5:00pm MT, November 18, 2010

Research paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than six pages (including the abstract, figures, tables, and references), double columned, 9-pt or 10-pt font, and (4) MUST NOT identify the author(s) by their name(s) or affiliation(s) anywhere on the manuscript or abstract, with all references to the author(s)'s own previous work or affiliations in the bibliographic citations being in the third person. The submitter must list all authors and their affiliations in the web-based submission form (i.e., not in the paper); the addition of new authors to an accepted paper will not be permitted. DAC papers go through a double blind review process; i.e., the identity of the authors and reviewers is only known to the TPC co-chairs. DAC must ensure that there are no conflicts of interest between the authors and the reviewers. Preliminary submissions will be at a disadvantage.
Format templates are available on the DAC website. Submissions not adhering to these rules will be rejected. DAC will compare each submission against a vast database and any paper with significant similarity to previously published works or with papers that are simultaneously under review with other venues with archival publications (e.g., conferences, symposia, journals, and workshops with archival proceedings), will be rejected. All research papers will be reviewed as finished papers. Authors of accepted papers must sign a copyright release form for their paper. Acceptance notices will be available by logging in to the DAC website after February 17, 2011. Complete author kits will be available on the DAC website by March 7, 2011. All conference presenters will be required to register at the time of final paper submission, present their paper and participate in a poster session.

USER TRACK PAPERS - EXTENDED ABSTRACTS

DUE BEFORE 5:00pm MT, January 11, 2011

DAC's User Track addresses the real-life issues facing IC designers, application engineers, and design flow developers. It provides valuable insights and experiences with in-house or commercial EDA tool flows. User Track papers may describe the application of EDA tools to the design of a novel electronic system, or the integration of EDA tools within a design flow or methodology to produce such systems. A User Track paper may be problem-specific in scope (e.g., analyzing substrate coupling during floorplanning) or may address a specific application domain (e.g., designing wireless handsets).
Initial submissions are in the form of a two page extended abstract. Final submissions will be in the form of a PowerPoint presentation. User Track authors will not be required to sign a copyright release form as final submissions will not be published. For more details, please see the separate User Track Call for Papers on the DAC website.

WILD AND CRAZY IDEAS (WACI) PAPERS

DUE BEFORE 5:00pm MT, November 18, 2010

The "Wild and Crazy Ideas" sessions cover interesting activities on a wide variety of topics that do not fit in the conventional mold. The WACI track features novel (and even preliminary or unproven) technical ideas. The aim of WACI is to promote revolutionary and way-out ideas that inspire discussion among conference attendees, create a buzz, and get people talking. Submissions to the WACI track should not exceed two pages, but must otherwise follow the above rules and deadlines for the research papers.
Unlike a DAC research paper that explores a specific technology problem and proposes a complete solution to it, with extensive experimental results, a WACI paper could present less developed but highly innovative ideas related to areas relevant to DAC. All WACI accepted papers will be required to post a two-minute video describing the work as part of the acceptance process.

SPECIAL SESSION SUGGESTIONS

DUE BEFORE 5:00pm MT, October 19, 2010

Special session suggestions must include descriptions of the proposed papers and speakers, and the importance of the special session to the DAC audience. A special session is devoted to a topic of strong contemporary or future interest. The topic must represent an emerging area that does not yet receive sufficient focus from research papers. A suggestion must list at least three inspiring speakers who address the topic from different angles. DAC reserves the right to restructure all special session suggestions.

PANEL AND TUTORIAL SUGGESTIONS

DUE BEFORE 5:00pm MT, October 19, 2010

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial suggestions. Please see the website for further details, or call the DAC office at +1-303-530-4333.

COLOCATED EVENT PROPOSALS

DUE BEFORE 5:00pm MT, January 20, 2011

DAC invites you to colocate your conference, meeting or other special event with DAC. We will provide you with meeting rooms at the conference center at no cost. Your event will be financed and otherwise organized by you. Please see the website for further details, or call the DAC office at +1-303-530-4333.

WORKSHOP SUBMISSIONS

DUE BEFORE 5:00pm MT, January 20, 2011

DAC invites you to organize a workshop on topics related to design, design methodologies, and design automation. DAC provides the financial and organizational support, including attendee registration, rooms at the conference center and audio visual equipment. Please see the website for further details, or call the DAC office at +1-303-530-4333.

STUDENT DESIGN CONTEST SUBMISSIONS

DUE BEFORE 5:00pm MT, November 12, 2010

ISSCC and DAC will jointly sponsor the 2011 ISSCC/DAC Student Design Contest. The contest promotes excellence in the design of electronic systems within an academic environment and provides a forum in which undergraduate/graduate students' ingenuity can be shared with an audience of academic/industrial technical experts. The winners will present their designs through a poster at ISSCC 2011 and DAC 2011. Designs can be for analog, digital, MEMS, optics, biological, or programmable circuits and embedded systems/platforms in any of the three categories: operational, system level, or conceptual. Please visit the DAC website for more details.

48TH CALL FOR CONTRIBUTIONS

SUBMISSION CATEGORIES FOR RESEARCH PAPERS

Authors of research papers are required to specify a category from the following list:

1. SYSTEM-LEVEL DESIGN AND CODESIGN

1.1 System specification, modeling, simulation, verification, and performance analysis
1.2 Scheduling, HW/SW partitioning, HW/SW interface synthesis
1.3 IP and platform-based design, IP protection
1.4 System-On-Chip (SOC) and multiprocessor System-On-Chip (MPSOC)
1.5 Application-specific processor design tools

2. SYSTEM-LEVEL COMMUNICATION AND NETWORKS-ON-CHIP

2.1 Modeling and performance analysis
2.2 Communications-based design, communication and network synthesis
2.3 Optimization for energy, fault tolerance, reliability
2.4 Interfacing and software issues, beyond-the-die communication
2.5 NOC design methodologies, case studies and prototyping

3. EMBEDDED HARDWARE DESIGN AND APPLICATIONS

3.1 Case studies of embedded system design
3.2 Flows and methods for specific applications and design domains
4. Embedded Software Tools and Design
4.1 Retargetable compilation
4.2 Memory/cache optimization
4.3 Software for single-/multiprocessor, multicore, GPU systems
4.4 Real-time operating systems
4.5 Verification of embedded software

5. POWER ANALYSIS AND LOW-POWER DESIGN

5.1 System-level power design and thermal management
5.2 Embedded low-power approaches: partitioning, scheduling, and resource management
5.3 High-level power estimation and optimization
5.4 Gate-level power analysis and optimization
5.5 Device and circuit techniques for lowpower
design
5.6 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies

6. VERIFICATION

6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
6.2 Dynamic simulation, equivalence checking, formal (and semiformal) verification model and property checking
6.3 Emulation and hardware simulators or accelerator engines
6.4 Modeling languages and related formalisms, verification plan development and implementation
6.5 Assertion-based verification, coverage analysis, constrained random testbench generation
6.6 Verification techniques for software correctness

7. HIGH-LEVEL SYNTHESIS, LOGIC SYNTHESIS AND CIRCUIT OPTIMIZATION

7.1 Combinational, sequential, and asynchronous logic synthesis
7.2 Library mapping, cell-based design and optimization
7.3 Transistor and gate sizing, resynthesis
7.4 Interactions between logic design and layout or physical synthesis
7.5 High-level, behavioral, algorithmic, and architectural synthesis, “C” to gates tools and methods
7.6 Resource scheduling, allocation, and synthesis

8. CIRCUIT, INTERCONNECT AND MANUFACTURING SIMULATION AND ANALYSIS

8.1 Electrical-level circuit simulation
8.2 Model order reduction methods for linear systems
8.3 Interconnect and substrate modeling and extraction
8.4 High-frequency and electromagnetic simulation of circuits
8.5 Thermal and electrothermal simulation
8.6 Technology CAD and fab automation

9. TIMING ANALYSIS

9.1 Process technology characterization, and modeling
9.2 Deterministic static timing analysis and verification
9.3 Statistical performance analysis and optimization

10. PHYSICAL DESIGN AND MANUFACTURABILITY

10.1 Floorplanning, partitioning, placement
10.2 Buffer insertion, routing, interconnect planning
10.3 Physical verification and design rule checking
10.4 Automated synthesis of clock networks
10.5 Reticle enhancement, lithographyrelated design optimizations
10.6 Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
10.7 Physical design of 3-D integrated circuits
10.8 System-in-package design, packageboard
codesign
10.9 Design for resilience under manufacturing variations

11. SIGNAL INTEGRITY AND DESIGN RELIABILITY

11.1 Signal integrity, capacitive and inductive crosstalk
11.2 Reliability modeling and analysis
11.3 Novel clocking and power delivery schemes
11.4 Power grid robustness analysis and optimization
11.5 Soft errors
11.6 Thermal reliability

12. ANALOG, MIXED-SIGNAL, AND RF

12.1 Analog, mixed-signal, and RF design methodologies
12.2 Automated synthesis
12.3 Analog, mixed-signal, and RF simulation
12.4 High-frequency design and advanced antenna design for wireless design

13. FPGA DESIGN TOOLS AND APPLICATIONS

13.1 Rapid prototyping
13.2 Logic synthesis and physical design techniques for FPGAs
13.3 Configurable and reconfigurable computing

14. TESTING

14.1 Test quality/reliability, current based test, delay test, low-power test
14.2 Digital fault modeling, automatic test generation, fault simulation
14.3 Digital design for test, test data compression, built-in self test
14.4 Memory test and repair, FPGA testing
14.5 Fault-tolerance and online testing
14.6 Analog/mixed-signal/RF testing, system-in-package (SIP) testing
14.7 Board- and system-level test, system-on-chip (SOC) testing
14.8 Silicon debug and diagnosis, postsilicon design validation

15. NEW AND EMERGING DESIGN TECHNOLOGIES (INCLUDING BUT NOT RESTRICTED TO)

15.1 MEMS, sensors, actuators, imaging devices
15.2 Nanotechnologies, nanowires, nanotubes
15.3 Quantum computing
15.4 Synthetic and systems biology, biologically-based or biologicallyinspired systems
15.5 Non-CMOS 3-D design, new transistor structures and devices, design in new or radical process technologies
15.6 Optical devices and communication

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEBSITE: WWW.DAC.COM.

ACM and IEEE reserve the right to exclude a paper from archival distribution after the conference if the paper is not presented at the conference, or in other exceptional cases.

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